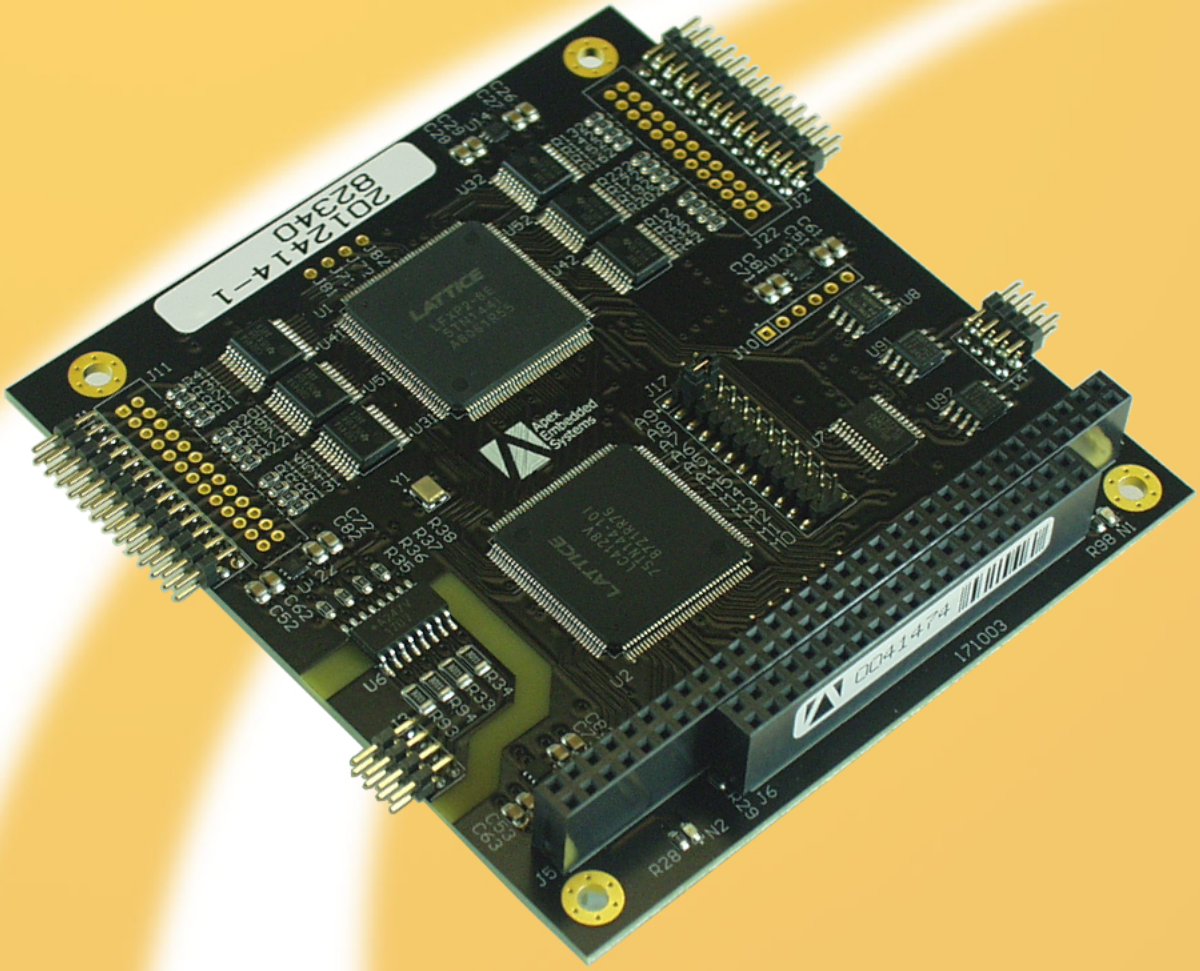
48 Channel DIO Card

48 channels of individually configurable DIO with 4 channels of high current outputs and 4 isolated inputs tied to a common return

Reference Manual



Apex Embedded Systems

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1 Welcome

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Continued Success,

Apex Embedded Systems

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3 Benfits and Features

3.1 Executive Summary

What is the Digtial I/O Card? The Digtial I/O Card is a 48-channel individually configurable DIO card, with 4 isolated inputs and 4 Power Digital Outputs.

Description

What are the Benefits of using the Digtial I/O Card? The Digtial I/O Card has the following benefits:

General Features

- Industrial temperature range from -40^{o}C to +85^{o}C
- Single +5V supply operation
- LED read/write status

Digital I/O features

- Individual channel direction control
- 5 Volt tolerant
- Sink 5V loads to 15mA per channel
- Source loads to 15mA per channel
- Outputs are LVTTL compatible
- 10K pull down resistors on all lines

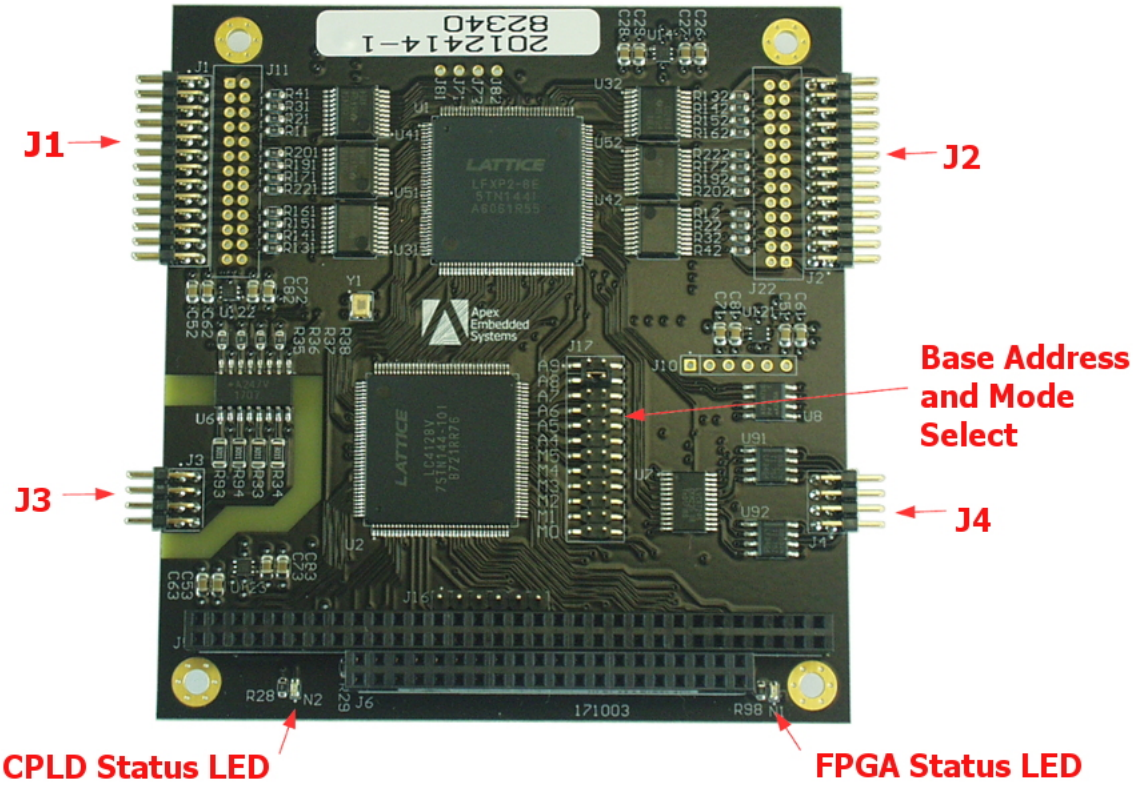
Isolated Inputs

- Activation Voltage from 4 - 13V
- Non-Activation Voltage 1.5V minimum
- Less than 5mA at 13V
- 500V Isolation
- Common ground among channels

High Current Outputs (Power Digital Outouts or PDO)

- Sink 1A @ 0.5V
- Load voltage 40V
- Common Ground

3.2 Photo


J1
J2
Base Address and Mode Select
J3
J4
CPLD Status LED
FPGA Status LED

4 ESD Caution

A discharge of static electricity from your hands can seriously damage certain electrical components on any circuit board. Before handling any board, discharge static electricity from yourself by touching a grounded conductor such as your computer chassis (your computer must be turned off). Whenever you handle a board, hold it by the edges and avoid touching any board components or cable connectors.

5 PC/104 Insertion Caution

Before powering up the PC/104 stack... 

and look for proper PC/104 connector alignment.

This simple step will prevent permanent board damage.

Helpful hint: During system prototyping install the spacers to help guide installation and provide another means of checking board alignment. We recommend having the bolt end of the spacer facing up to act as a guide or alignment pin.

6 Hardware Configuration

6.1 Base Address Table

Card Base Address set via installing jumpers at J6 positions A9, A8, A7, A6, A5 and A4. The allowable address range is 0x000 to 0x3F0. Examples of jumper arrangements are shown below.

Description

BASE ADDRESS	A9	A8	A7	A6	A5	A4
0x260	1	0	0	1	1	0
0x280	1	0	1	0	0	0
0x290	1	0	1	0	0	1
0x2A0	1	0	1	0	1	0
0x2B0	1	0	1	0	1	1
0x2C0	1	0	1	1	0	0
0x2D0	1	0	1	1	0	1
0x2E0	1	0	1	1	1	0
0x2F0	1	0	1	1	1	1
0x300*	1	1	0	0	0	0
0x310	1	1	0	0	0	1
0x320	1	1	0	0	1	0
0x330	1	1	0	0	1	1
0x340	1	1	0	1	0	0
0x350	1	1	0	1	0	1
0x360	1	1	0	1	1	0
0x370	1	1	0	1	1	1
0x380	1	1	1	0	0	0
0x390	1	1	1	0	0	1
0x3A0	1	1	1	0	1	0
0x3B0	1	1	1	0	1	1
0x3C0	1	1	1	1	0	0
0x3D0	1	1	1	1	0	1
0x3E0	1	1	1	1	1	0
0x3F0	1	1	1	1	1	1

Notes: 1 = Jumper installed, 0 = Jumper not installed.

* Factory Default

6.2 Interrupts

Interrupts can be set via installing jumpers at J17 positions M0, M1, M2, and M3. Input 0 of the Isolated inputs can be routed as an interrupt. The interrupt will be active the entire time the the input is high.

Description

Interrupt	M3	M2	M1	M0
IRQ3	0	0	1	1
IRQ4	0	1	0	0
IRQ5	0	1	0	1
IRQ6	0	1	1	0
IRQ7	0	1	1	1
IRQ9/2	1	0	0	1
IRQ10	1	0	1	0
IRQ11	1	0	1	1
IRQ12	1	1	0	0
IRQ14	1	1	1	0
IRQ15	1	1	1	1

Notes: 1 = Jumper installed, 0 = Jumper not installed.

* Factory Default

7 Register Set

7.1 Summary

Overview of the Digtial I/O Card register set.

Description

Register Name	Direction	Offset	M5
DIO Port 1 A (see page 9)	rw	0	X
DIO Port 1 B (see page 10)	rw	1	X
DIO Port 1 C (see page 11)	rw	2	X
DIO Port 1 Control Register (see page 12)	w	3	X
DIO Port 2 A (see page 13)	rw	4	X
DIO Port 2 B (see page 14)	rw	5	X
DIO Port 2 C (see page 15)	rw	6	X
DIO Port 2 Control Register (see page 15)	w	7	X
High Current Output 0 (see page 16)	rw	8	X
High Current Output 1 (see page 17)	rw	9	X
High Current Output 2	rw	10	X
High Current Output 3 (see page 18)	rw	11	X
FPGA Data (see page 19)	r	12	1
FPGA Index (see page 19)	rw	13	1
Reserved for Apex	-	14	-
Scratch Pad	rw	15	1

Note: Registers with a "1" in the M5 column will only be available when jumper M5 is installed. Registers with an "X" are available at any time.

Example

7.2 DIO Port 1 A (Offset=0)

Port 1 A DIO Register.

Description

Register Layout **Offset=0x0**

D7	D6	D5	D4	D3	D2	D1	D0
D1A7	D1A6	D1A5	D1A4	D1A3	D1A2	D1A1	D1A0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
D1A[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=3) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=3) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=3) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.3 DIO Port 1 B (Offset=1)

Port 1 B DIO Register.

Description

Register Layout **Offset=0x1.**

D7	D6	D5	D4	D3	D2	D1	D0
D1B7	D1B6	D1B5	D1B4	D1B3	D1B2	D1B1	D1B0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
D1B[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=3) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=3) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=3) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.4 DIO Port 1 C (Offset=2)

Port 1 C DIO Register.

Description

Register Layout **Offset=0x2.**

D7	D6	D5	D4	D3	D2	D1	D0
D1C7	D1C6	D1C5	D1C4	D1C3	D1C2	D1C1	D1C0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care

D1C[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=3) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=3) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=3) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.5 DIO Port 2 Control Register (Offset = 3)

Port 1 Control Register.

Description

Register Layout **Offset=0x3.**

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	P1CR1	P1CR0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care. To be compatible with any future upgrades please set these as 0
P1CR[1:0]	r/w	0x03	Mode 0x01 - Preset Mode 0x02 - Direction Mode 0x03 - Operation Mode

Setting the value of this register will allow you to control the mode of the port 1 data registers.

Please Note: When this register is in Preset Mode (0x01), the values written to the port registers are updated **immediately**. When this register is set to Direction Mode(0x02), the values written to the port register will update the direction **immediately**. This was done to match the functionality of the Octagon Board.

See Also

Register Summary (see page 9)

Example

7.6 DIO Port 2 A (Offset=4)

Port 2 A DIO Register.

Description

Register Layout **Offset=0x4**

D7	D6	D5	D4	D3	D2	D1	D0
D2A7	D2A6	D2A5	D2A4	D2A3	D2A2	D2A1	D2A0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
D2A[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=7) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=7) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=7) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.7 DIO Port 2 B (Offset=5)

Port 2 B DIO Register.

Description

Register Layout **Offset=0x5.**

D7	D6	D5	D4	D3	D2	D1	D0
D2B7	D2B6	D2B5	D2B4	D2B3	D2B2	D2B1	D2B0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
D2B[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=7) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=7) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=7) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.8 DIO Port 2 C (Offset=6)

Port 2 C DIO Register.

Description

Register Layout **Offset=0x6.**

D7	D6	D5	D4	D3	D2	D1	D0
D2C7	D2C6	D2C5	D2C4	D2C3	D2C2	D2C1	D2C0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
D2C[7:0]	r/w	00	Control Register set to Preset (0x01) 0 - Output low 1 - Output High Control Register set to Direction (0x02) 0 - Input 1 - Output Control Register set to Operation (0x03) 0 - Output low 1 - Output High Reading will report the values set for the corresponding mode. When in Operation mode, reading will return the values of the inputs and the values of any bits that have been set to outputs.

Writing to this register when the Control Register (offset=7) is set to 0x01, will **immediately** set the values of the outputs. Bits set as inputs will not be affected. Reading will report the the value written regardless of how the direction is set. Writing to this register when the Control Register (offset=7) is set to 0x02, will **immediately** set the direction. Reading back will report the direction that is set. Writing to this register when the Control Register (offset=7) is set to 0x03, will **immediately** set the value output bits. Bits set as inputs will not be affected. Reading will report back the value of the input or the set value of the output.

See Also

Register Summary (see page 9)

Example

7.9 DIO Port 2 Control Register (Offset=7)

Port 2 Control Register.

Description

Register Layout **Offset=0x3.**

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	P2CR1	P2CR0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care. To be compatible with any future upgrades please set these as 0
P2CR[1:0]	r/w	0x03	Mode 0x01 - Preset Mode 0x02 - Direction Mode 0x03 - Operation Mode

Setting the value of this register will allow you to control the mode of the port 2 data registers.

Please Note: When this register is in Preset Mode (0x01), the values written to the port registers are updated **immediately**. When this register is set to Direction Mode(0x02), the values written to the port register will update the direction **immediately**. This was done to match the functionality of the Octagon Board.

See Also

Register Summary (see page 9)

Example

7.10 High Current Output 0 (Offset=8)

High Current Output 0 and Isolated Inputs

Description

Register Layout **Offset=0x8**

D7	D6	D5	D4	D3	D2	D1	D0
IN3	IN2	IN1	IN0	OUT3	OUT2	OUT1	OUT0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
IN[3:0]	r	-	Isolated Inputs.
OUT[3:0]	r	-	When read, this register returns the Inverted value of what was written.

OUT0	w	0	Sets the output for Hight Current Output 0 0 - Off 1 - On

Input 0 of the Isolated inputs can be routed as an interrupt. The interrupt will be active the entire time the the input is high. (See Interrupts (see page 8))

This register can read all 4 isolated inputs and the status of all 4 High Current Outputs but it can only set High Current Output 0.

See Also

Register Summary (see page 9)

Example

7.11 High Current Output 1 (Offset=9)

High Current Output 1 and Isolated Inputs

Description

Register Layout **Offset=0x9**

D7	D6	D5	D4	D3	D2	D1	D0
IN3	IN2	IN1	IN0	OUT3	OUT2	OUT1	OUT0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
IN[3:0]	r	-	Isolated Inputs.
OUT[3:0]	r	-	When read, this register returns the Inverted value of what was written.
OUT1	w	0	Sets the output for Hight Current Output 1 0 - Off 1 - On

Input 0 of the Isolated inputs can be routed as an interrupt. The interrupt will be active the entire time the the input is high. (See Interrupts (see page 8))

This register can read all 4 isolated inputs and the status of all 4 High Current Outputs but it can only set High Current Output 1.

See Also

Register Summary (see page 9)

Example

7.12 High Current Output 2 (Offset=10)

High Current Output 2 and Isolated Inputs

Description

Register Layout **Offset=0xA**

D7	D6	D5	D4	D3	D2	D1	D0
IN3	IN2	IN1	IN0	OUT3	OUT2	OUT1	OUT0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
IN[3:0]	r	-	Isolated Inputs.
OUT[3:0]	r	-	When read, this register returns the Inverted value of what was written.
OUT2	w	0	Sets the output for Hight Current Output 2 0 - Off 1 - On

Input 0 of the Isolated inputs can be routed as an interrupt. The interrupt will be active the entire time the the input is high. (See Interrupts (see page 8))

This register can read all 4 isolated inputs and the status of all 4 High Current Outputs but it can only set High Current Output 0.

See Also

Register Summary (see page 9)

Example

7.13 High Current Output 3 (Offset=11)

High Current Output 3 and Isolated Inputs

Description

Register Layout **Offset=0xB**

D7	D6	D5	D4	D3	D2	D1	D0
IN3	IN2	IN1	IN0	OUT3	OUT2	OUT1	OUT0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
X	-	-	Don't Care
IN[3:0]	r	-	Isolated Inputs.
OUT[3:0]	r	-	When read, this register returns the Inverted value of what was written.
OUT3	w	0	Sets the output for Hight Current Output 3 0 - Off 1 - On

Input 0 of the Isolated inputs can be routed as an interrupt. The interrupt will be active the entire time the the input is high. (See Interrupts (see page 8))

This register can read all 4 isolated inputs and the status of all 4 High Current Outputs but it can only set High Current Output 0.

See Also

Register Summary (see page 9)

Example

7.14 FPGA Information (Offset= 12-13)

FPGA date time information data memory. To access this mode jumper M5 must be placed.

Description

FPGA date time information data memory. This currently contains both the subversion (SVN) date stamp as well as the last compilation date of the FPGA (which is likely a later date). The data is embedded in an indexed read only memory structure. The definition of the memory is illustrated below. Register Layout

FPGA Data Register: Offset = 0xC, M5 = Installed, Read Only.

D7	D6	D5	D4	D3	D2	D1	D0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

FPGA Index Register: Offset =0xD, M5 = Installed, Read/Write

D7	D6	D5	D4	D3	D2	D1	D0
FI7	FI6	FI5	FI4	FI3	FI2	FI1	FI0

Notes:

1. "CT_" is short for Compilation Time.
2. "SVN_" is short for SubVersioN date time stamp. Subversion is a revision control software
3. The read only memory structure is arranged into a very simple data structure allowing for future revisions as well as potential arbitrary length chunks of information.

4. All time stamp information is in a decimal format of YYmmddHHMM where "YY" is the last 2-digits of the year, "mm" is month, "dd" is the day, "HH" is the hour (24-hour format), "MM" is the minutes.
5. The intent of the data structure is to allow for expansion in a limited way.

Register set definition

Index (FI)	Data (FD)	Register Description
0	0x06	Absolute index address to next data structure
1	'S'	Data structure type, in this case it is a Subversion (SVN) time stamp composed of four bytes in a 32-bit unsigned decimal format. See note #4 above.
2	SVN_Date_Byte0	Least significant byte
3	SVN_Date_Byte1	
4	SVN_Date_Byte2	
5	SVN_Date_Byte3	Most significant byte
6	0x0C	Absolute index address to next data structure
7	'C'	Data structure type, in this case it is a compilation time stamp composed of four bytes in a 32-bit unsigned decimal format. See note #4 above.
8	CT_Date_Byte0	Least significant byte
9	CT_Date_Byte1	
10	CT_Date_Byte2	
11	CT_Date_Byte3	Most significant byte
12	0x0F	Absolute index address to next data structure
13	'C'	Data structure type, in this case it is Firmware ID composed of an 8-bit unsigned decimal.
14	Firmware_ID	
15	0xFF	Data structure type, in this case it is a 'terminate' meaning end of data.

See Also

Register Summary (see page 9)

Example

```
unsigned int base_address_uut = 0x300;
int index;
uint8 dt [16];

/* read all date and time registers*/
for ( index = 0; index < 16; index++ )
{
    output(base_address_uut + 0x0D,index)
    dt[index] = inp(base_address_uut + 0xC);
}

printf(" Firmware Information in Hex \n");
/* print all date and time values*/
for ( index = 15; index .>= 0; index-- )
{
    printf("%X ", dt[index]);
}
printf("\n");
```

7.15 Scratch Pad (Offset=15)

Scratch Pad Register

Description

Can be used to verify ISA bus interface. Also could be used for temporarily storing a value but this is not recommended, as this register will be allocated for another use in a future revision of firmware.

Register Layout **Offset=0xF, M5=Installed**

D7	D6	D5	D4	D3	D2	D1	D0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

Bit Definitions

NAME	DIRECTION	DEFAULT	DESCRIPTION
SCR[7:0]	rw	0x00	Scratch Pad Register

See Also

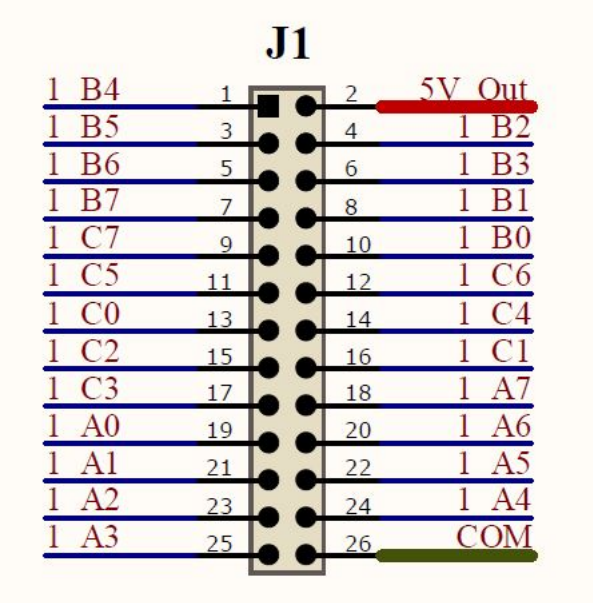
Register Summary (see page 9)

Example

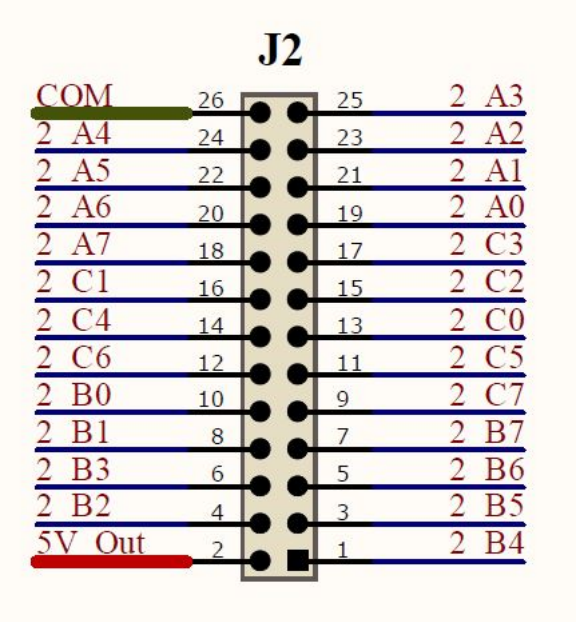
8 Connector Summary

Description

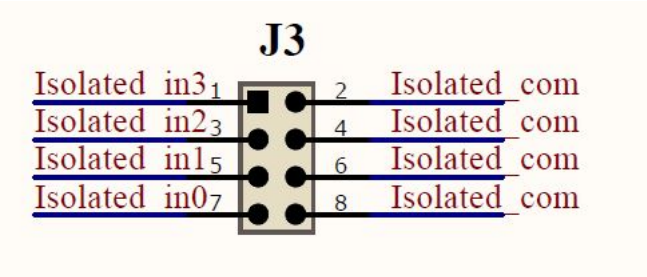
DIO Connector J1



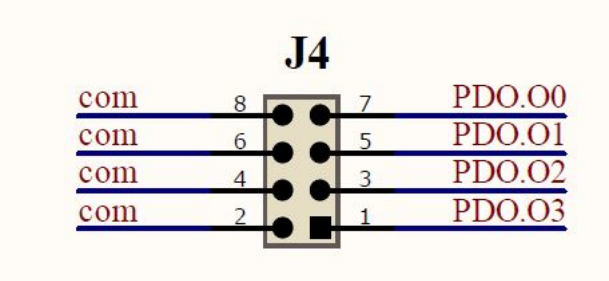
DIO Connector J2



Isolated Input Connector J3



High Current Output(PDO) Connector J4



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