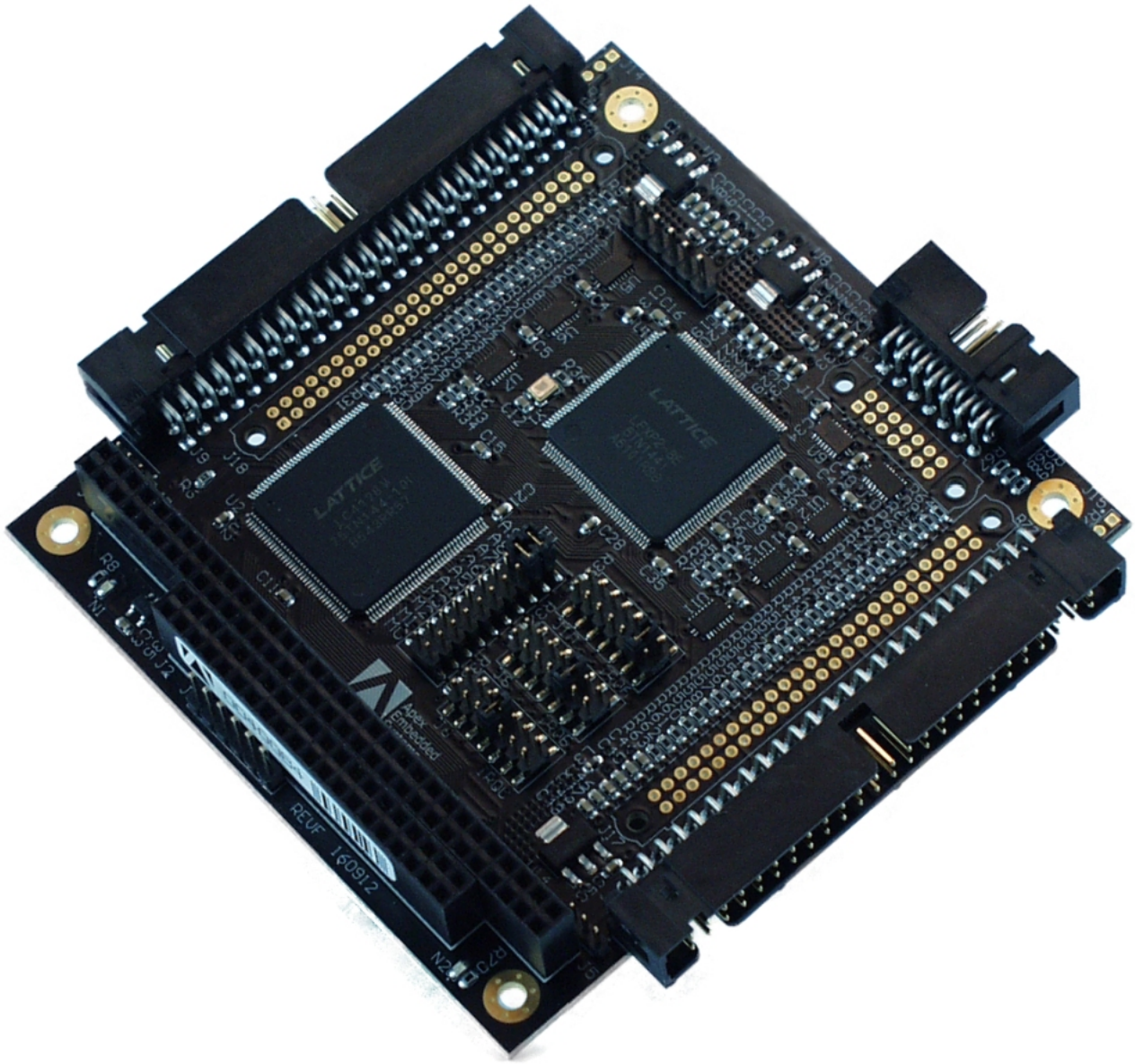
Tracer Reference Manual

48 Channel Digital I/O with three 16 bit counter timers



Apex Embedded Systems

Tracer Reference Manual

RUGGEDIZED COTs PC/104 High Drive 48-line DIO and counter-timer module

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Tracer Reference Manual

1 Welcome

Dear Valued Customer:

Thank you for your interest in our products and services.

Apex Embedded Systems "Continuous improvement" policy utilizes customer feedback to improve existing products and create new product offerings based on needs of our customers.

Continued Success,

Apex Embedded Systems LLC

2 Legal Notice

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This warranty does not apply to products which have been subject to misuse (including static discharge), neglect, accident or modification, or which have been soldered or altered during assembly and are not capable of being tested.

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Products sold by Apex Embedded Systems are not authorized for use as critical components in life support devices or systems. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

3 Benefits and Features

3.1 Exective Summary

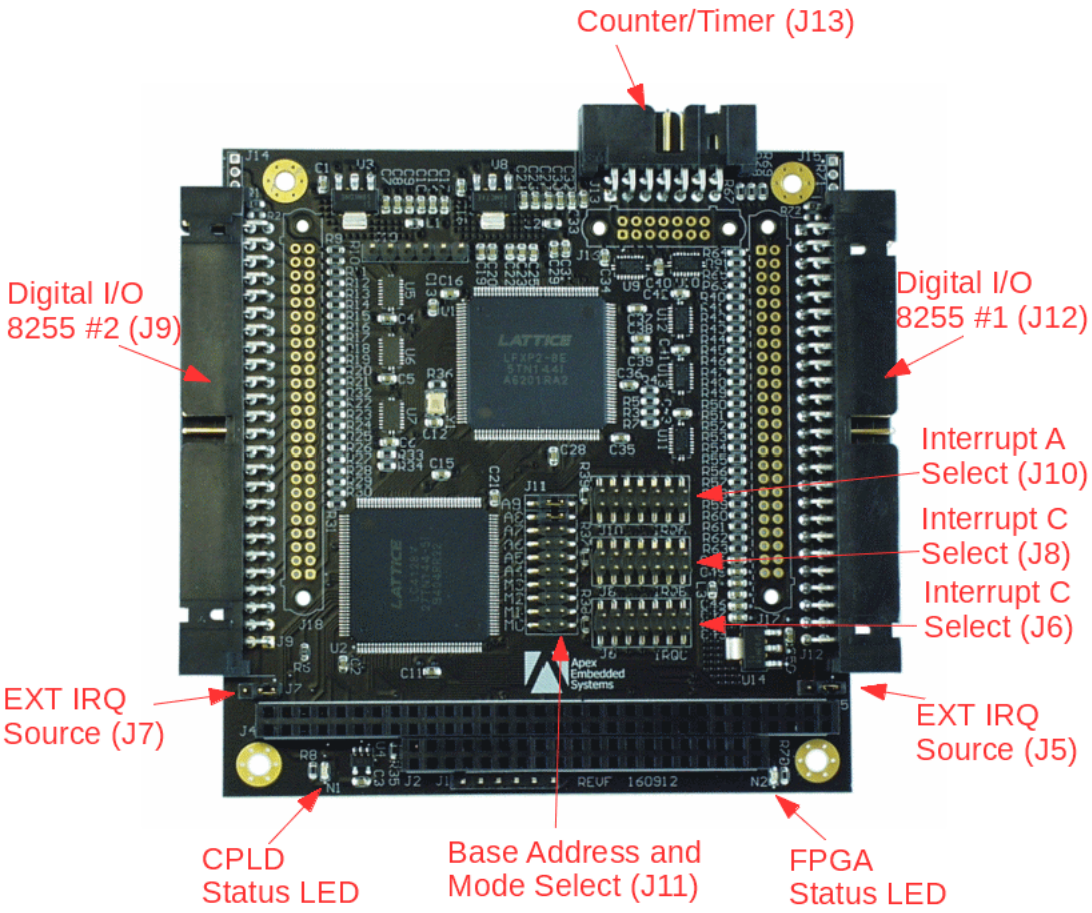
What is the Tracer? The Tracer is a standard digital I/O card utilizing 8255 style software interfacing. In addition, an 8254 counter/timer function is available for general use.

Description

What are the Benefits of using the Tracer? The Tracer has the following benefits:

- Digital I/O connectors organized to allow direct interfacing to OPTO-22's isolated I/O racks including the G4 series, the PB16-H, PB16-J, PB16-K, PB16-L, PB8H and the PB24HQ. All that is required is a 50-pin ribbon cable from the Tracer to any of the OPTO-22 racks.
- High current capacity sinking 32mA on each digital output
- Broad selection of interrupt sources and software configurable.
- On-board LED to indicate general status and useful for system debugging. A wide variety of signals can be routed to the LED via software selection.
- 8254 Counter/Timer operation to 40 MHz
- Counter/Timer can be easily configured to support quadrature encoder signals, see application note (see page 35).
- Industrial temperature range from -40^{o}C to +85^{o}C
- No tantalum capacitors or electrolytic capacitors used in the design

3.2 Photo


Counter/Timer (J13)
Digital I/O
8255 #2 (J9)
Digital I/O
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EXT IRQ
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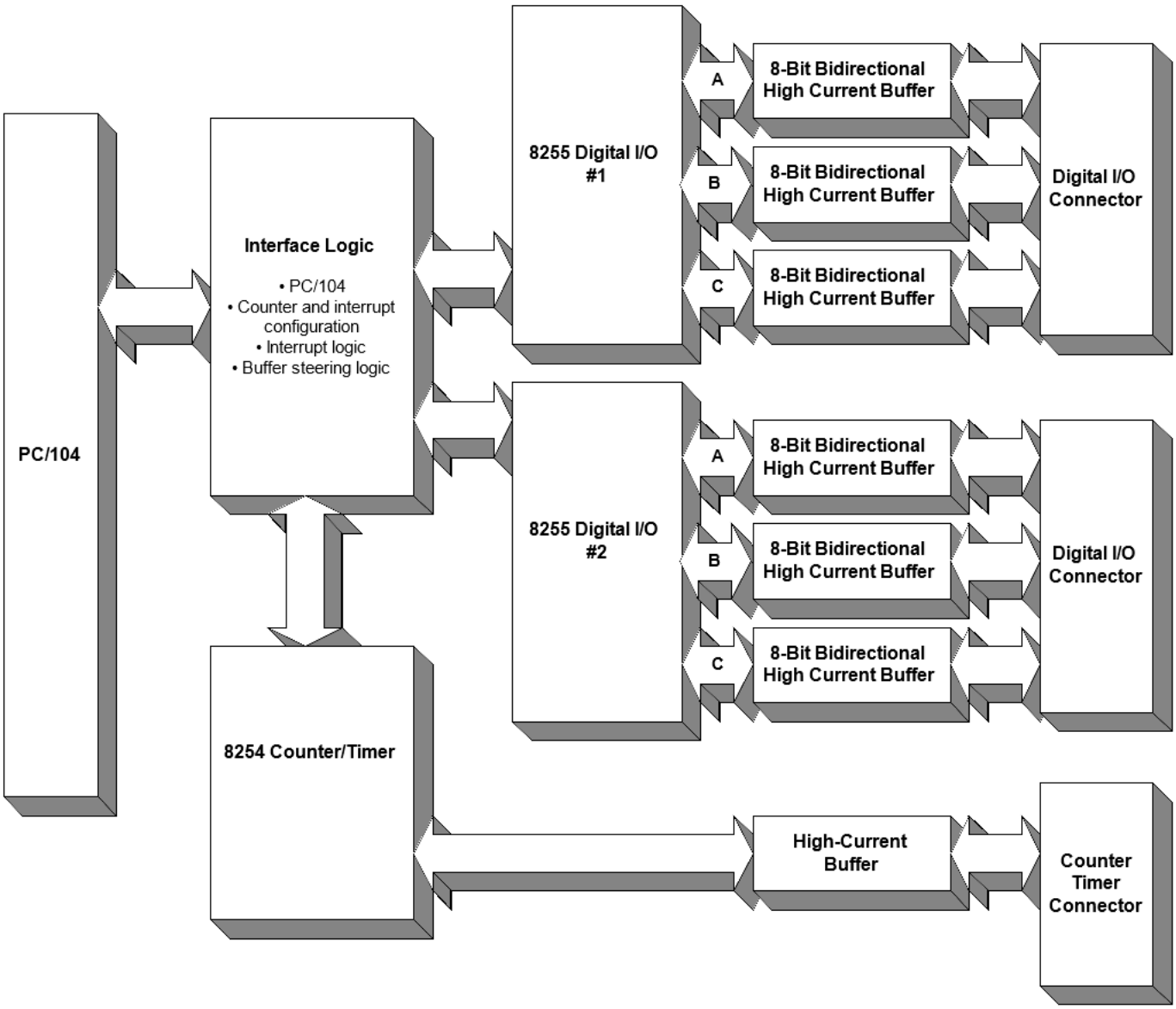
Status LED
Base Address and
Mode Select (J11)
FPGA
Status LED

3.3 Tracer Block Diagram



4 Errata

Addresses known board related issues and includes methods to work around the issues.

Description

Please refer to updated specifications (see page 29) and switch input pull-up requirements.

--- end

5 ESD Caution

A discharge of static electricity from your hands can seriously damage certain electrical components on any circuit board. Before handling any board, discharge static electricity from yourself by touching a grounded conductor such as your computer chassis (your computer must be turned off). Whenever you handle a board, hold it by the edges and avoid touching any board components or cable connectors.

6 PC/104 Insertion Caution

Before powering up the PC/104 stack... 

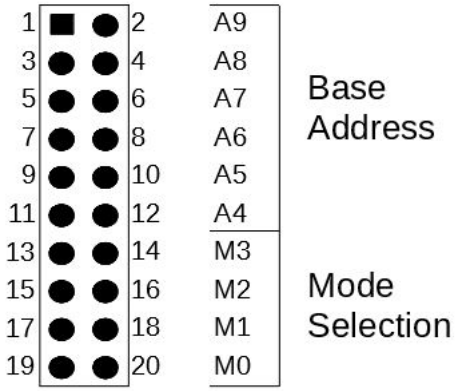
and look for proper PC/104 connector alignment.

This simple step will prevent permanent board damage.

Helpful hint: During system prototyping install the spacers to help guide installation and provide another means of checking board alignment. We recommend having the bolt end of the spacer facing up to act as a guide or alignment pin.

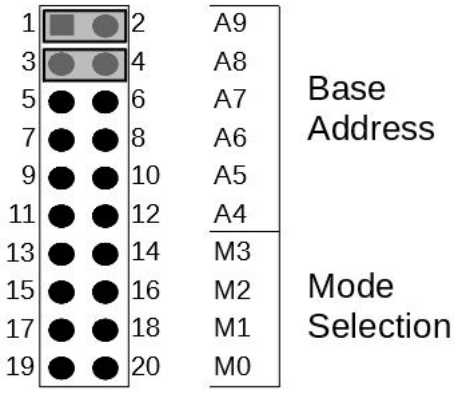
7 Hardware Configuration

7.1 Base Address and Configuration



Example Base Address

Base Address = 768 or 0x300 (11 0000 0000_2)



Mode	M3	M2	M1	M0
Normal, Legacy*	0	0	0	0
J12.9 replaces J13.2 (J12.9 will now be CT_CLK1)	0	1	0	0

Note: 1 = Jumper installed 0 = Jumper not installed

*Factory Default

7.2 Base Address Table

Card Base Address set via installing jumpers at J11 positions A9, A8, A7, A6, A5 and A4.

Description

BASE ADDRESS	A9	A8	A7	A6	A5	A4
0x220	1	0	0	0	1	0
0x240	1	0	0	1	0	0
0x250	1	0	0	1	0	1
0x260	1	0	0	1	1	0
0x280	1	0	1	0	0	0
0x290	1	0	1	0	0	1
0x2A0	1	0	1	0	1	0
0x2B0	1	0	1	0	1	1
0x2C0	1	0	1	1	0	0
0x2D0	1	0	1	1	0	1
0x2E0	1	0	1	1	1	0
0x2F0	1	0	1	1	1	1
0x300*	1	1	0	0	0	0
0x310	1	1	0	0	0	1
0x320	1	1	0	0	1	0
0x330	1	1	0	0	1	1
0x340	1	1	0	1	0	0
0x350	1	1	0	1	0	1
0x360	1	1	0	1	1	0
0x370	1	1	0	1	1	1
0x380	1	1	1	0	0	0
0x390	1	1	1	0	0	1
0x3A0	1	1	1	0	1	0
0x3B0	1	1	1	0	1	1
0x3C0	1	1	1	1	0	0
0x3D0	1	1	1	1	0	1
0x3E0	1	1	1	1	1	0
0x3F0	1	1	1	1	1	1

Notes: 1 = Jumper installed, 0 = Jumper not installed.

* Factory Default

Apex offers factory configured hard-coded jumper settings for high vibration requirements. Resistors are soldered to the board in place of jumpers to insure successful operation in high vibration conditions.

8 Register Set

8.1 Summary

Register Name	Direction	Offset Decimal	Index (Hex)
8255 Device #1 Port A Register (see page 12)	Read/Write	0	-
8255 Device #1 Port B Register (see page 12)	Read/Write	1	-
8255 Device #1 Port C Register (see page 12)	Read/Write	2	-
8255 Device #1 Configuration Register (see page 12)	Write	3	-
8255 Device #2 Port A Register (see page 15)	Read/Write	4	-
8255 Device #2 Port B Register (see page 15)	Read/Write	5	-
8255 Device #2 Port C Register (see page 15)	Read/Write	6	-
8255 Device #2 Configuration Register (see page 15)	Write	7	-
8254 Counter/Timer 0 Data (see page 18)	Read/Write	8	-
8254 Counter/Timer 1 Data (see page 18)	Read/Write	9	-
8254 Counter/Timer 2 Data (see page 18)	Read/Write	10	-
8254 Counter/Timer Mode Configuration Register (see page 18)	Write	11	-
8254 Counter/Timer Input Setup Low Byte Register (see page 19)	Read/Write	12	-
8254 Counter/Timer Input Setup High Byte Register (see page 19)	Read/Write	13	-
General Setup Low Byte Register (see page 22)	Read/Write	14	-
General Setup High Byte Register (see page 22)	Read/Write	15	-

8.2 8255 Device #1 Registers

Detailed register information for 8255 device #1. Both bit names and associated connector placement are shown where applicable (i.e. ref.pin#).

Base + 0 **8255 Device #1 Port A Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1A7	1A6	1A5	1A4	1A3	1A2	1A1	1A0

Associated Connector Pins:

J12.1	J12.3	J12.5	J12.7	J12.9	J12.11	J12.13	J12.15

Base + 1 **8255 Device #1 Port B Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0

Associated Connector Pins:

J12.33	J12.35	J12.37	J12.39	J12.41	J12.43	J12.45	J12.47

Base + 2 **8255 Device #1 Port C Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1C7	1C6	1C5	1C4	1C3	1C2	1C1	1C0

Associated Connector Pins:

J12.17	J12.19	J12.21	J12.23	J12.25	J12.27	J12.29	J12.31

Base + 3 **8255 Device #1 Configuration Register** **Write**

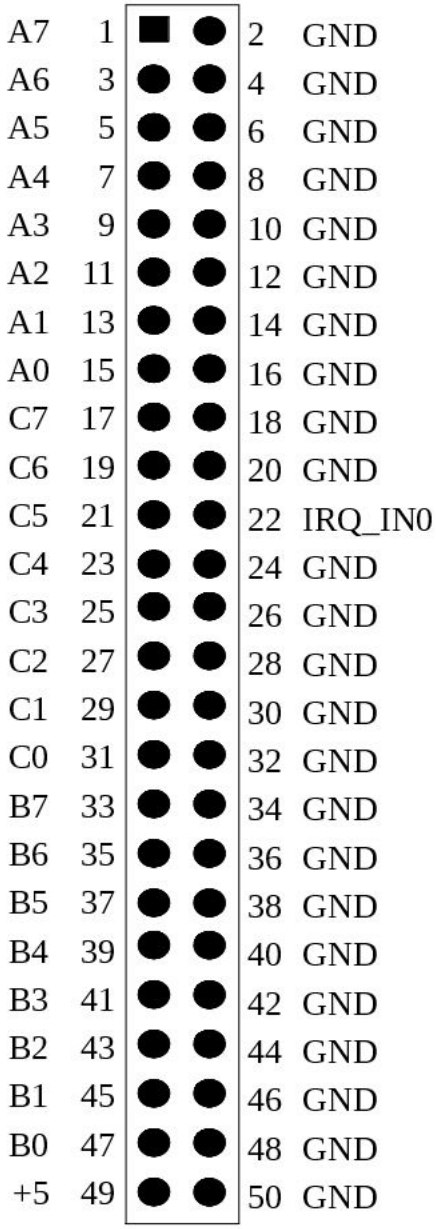
D7	D6	D5	D4	D3	D2	D1	D0
	Group A	Group A	Group A	Group A	Group B	Group B	Group B
Mode Set	M3	M2	A	CH	M1	B	CL

8255 Configuration codes valid for the Tracer. Only Mode 0 is supported.

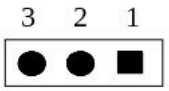
Port Direction A	Port Direction CH	Port Direction CL	Port Direction B	Hex Value	Decimal Value
IN	IN	IN	IN	0x9B	155
IN	IN	IN	OUT	0x99	153
IN	OUT	OUT	IN	0x92	146
IN	OUT	OUT	OUT	0x90	144
OUT	IN	IN	IN	0x8B	139
OUT	IN	IN	OUT	0x89	137
OUT	OUT	OUT	IN	0x82	130
OUT	OUT	OUT	OUT	0x80	128

8.3 Digital I/O Connector J12, 8255 #1

J12



8.4 External IRQ Source 0 (IRQ_IN0) J5



J5

Jumper Position	Function
1-2	External Interrupt source 0 input at J12 pin 22 (J12.22)
2-3*	J12 pin 22 grounded (for opto 22 rack compatibility). External Interrupt Source 0 not available.

* FACTORY CONFIGURATION

8.5 8255 Device #2 Registers

Detailed register information for 8255 device #2. Both bit names and associated connector placement are shown where applicable (i.e. ref.pin#).

Base + 4 **8255 Device #2 Port A Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
2A7	2A6	2A5	2A4	2A3	2A2	2A1	2A0

Associated Connector Pins:

J9.1	J9.3	J9.5	J9.7	J9.9	J9.11	J9.13	J9.15

Base + 5 **8255 Device #2 Port B Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
2B7	2B6	2B5	2B4	2B3	2B2	2B1	2B0

Associated Connector Pins:

J9.33	J9.35	J9.37	J9.39	J9.41	J9.43	J9.45	J9.47

Base + 6 **8255 Device #2 Port C Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
2C7	2C6	2C5	2C4	2C3	2C2	2C1	2C0

Associated Connector Pins:

J9.17	J9.19	J9.21	J9.23	J9.25	J9.27	J9.29	J9.31

Base + 7 **8255 Device #2 Configuration Register** **Write**

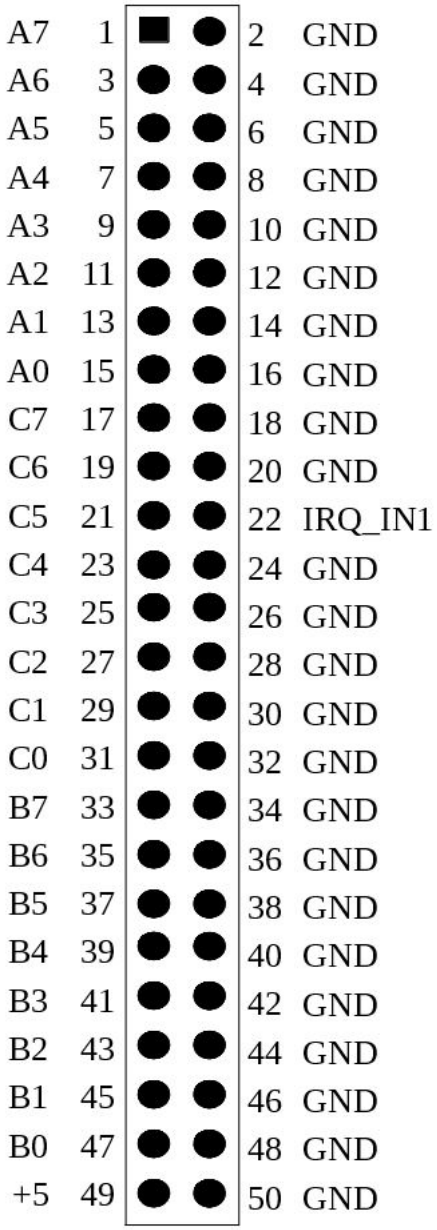
D7	D6	D5	D4	D3	D2	D1	D0
	Group A	Group A	Group A	Group A	Group B	Group B	Group B
Mode Set	M3	M2	A	CH	M1	B	CL

8255 Configuration codes valid for the Tracer. Only Mode 0 is supported.

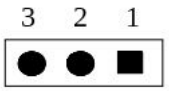
Port Direction A	Port Direction CH	Port Direction CL	Port Direction B	Hex Value	Decimal Value
IN	IN	IN	IN	0x9B	155
IN	IN	IN	OUT	0x99	153
IN	OUT	OUT	IN	0x92	146
IN	OUT	OUT	OUT	0x90	144
OUT	IN	IN	IN	0x8B	139
OUT	IN	IN	OUT	0x89	137
OUT	OUT	OUT	IN	0x82	130
OUT	OUT	OUT	OUT	0x80	128

8.6 Digital I/O Connector J9, 8255 #2

J9



8.7 External IRQ Source 1 (IRQ_IN1) J7



J7

Jumper Position	Function
1-2	External Interrupt source 1 input at J9 pin 22 (J9.22)
2-3*	J9 pin 22 grounded (for opto 22 rack compatibility). External Interrupt Source 1 not available.

* FACTORY CONFIGURATION

8.8 8254 Counter/Timer Registers

Data registers to/from the each of the three counter/timers.

Base + 8 **8254 Counter/Timer 0 Data** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Base + 9 **8254 Counter/Timer 1 Data** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Base + 10 **8254 Counter/Timer 2 Data** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Base + 11 **8254 Counter/Timer Mode Configuration Register** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

BCD = Binary Coded Decimal (BCD) Counter (4 decades) if set to one, otherwise 16-bit binary counter.

M[2:0] = Counter/Timer Mode Select:

000 = Mode 0, Interrupt on terminal count
001 = Mode 1, Hardware retriggerable one-shot
X10 = Mode 2, Rate generator
X11 = Mode 3, Square wave generator
100 = Mode 4, Software triggered strobe
101 = Mode 5, Hardware triggered strobe (retriggerable)

RW[1:0] = Read/Write:

00 = Counter latch command
01 = Read/Write least significant byte only
10 = Read/Write most significant byte only
11 = Read/Write least significant byte first, then most significant byte.

SC[1:0] = Select Counter:

00 = Select Counter 0
01 = Select Counter 1
10 = Select Counter 2
11 = Read-Back Command (see read operations)

8.9 Counter/Timer Setup Registers

Base + 12 **8254 Counter/Timer input Setup Low Byte Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
CLK1_INV	CLK12	CLK11	CLK10	CLK0_INV	CLK02	CLK01	CLK00

Base + 13 **8254 Counter/Timer input Setup High Byte Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
GT0	GT2_INV	GT1_INV	GT0_INV	CLK_INV	CLK22	CLK21	CLK20

GT2_INV = Counter #2 gate input polarity:

0 = clock input non-inverted (default)
1 = clock input inverted

CLK2_INV = Counter #2 clock input polarity:

0 = clock input non-inverted (default)
1 = clock input inverted

CLK2[2:0] = Counter #2 clock input selection:

000 = CT_IN2 (default)
001 = CT_OUT0
010 = CT_OUT1
011 = IRQ_IN2
100 = 4 MHz oscillator
101 = 10 MHz oscillator
110 = 20 MHz oscillator
111 = 40 MHz oscillator

GT1_INV = Counter #1 gate input polarity:

0 = clock input non-inverted (default)
1 = clock input inverted

CLK1_INV = Counter #1 clock input polarity:

0 = clock input non-inverted (default)
1 = clock input inverted

CLK1[2:0] = Counter #1 clock input selection:

000 = CT_IN1 (default)
001 = CT_OUT0
010 = CT_OUT2
011 = IRQ_IN2
100 = 4 MHz oscillator
101 = 10 MHz oscillator
110 = 20 MHz oscillator
111 = 40 MHz oscillator

GT0_INV = Counter #0 gate input polarity:

0 = clock input non-inverted (default)
1 = clock input inverted

GT0 = Counter #0 gate input selection:

0 = CT_GATE0 (default)
1 = CT_GATE1

CLK0_INV = Counter #0 clock input polarity:

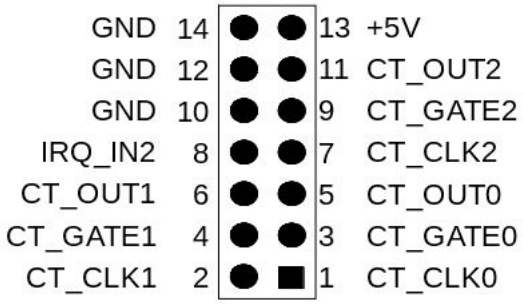
0 = clock input non-inverted (default)
1 = clock input inverted

CLK0[2:0] = Counter #0 clock input selection:

000 = CT_IN0 (default)
001 = CT_IN1
010 = CT_OUT2
011 = IRQ_IN2
100 = 4 MHz oscillator
101 = 10 MHz oscillator
110 = 20 MHz oscillator
111 = 40 MHz oscillator

8.10 Counter/Timer I/O Connector J13

Counter/Timer connector J13:



Name	Direction
CT_CLK0	Input to Tracer Board
CT_GATE0	Input to Tracer Board
CT_OUT0	Output from Tracer Board
CT_CLK1	Input to Tracer Board
CT_GATE1	Input to Tracer Board
CT_OUT1	Output from Tracer Board
CT_CLK2	Input to Tracer Board
CT_GATE2	Input to Tracer Board
CT_OUT2	Output from Tracer Board

IRQ_IN2	Additional interrupt input

8.11 General Configuration Register

RB = 0: Offset = Base + 14

General Setup Low Byte Register **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
IEB	ISB2	ISB1	ISB0	IEA	ISA2	ISA1	ISA0

RB = 0: Offset = Base + 15

General Setup High Byte Register **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
LED3	LED2	LED1	LED0	IEC	ISC2	ISC1	ISC0

8

IEA = Interrupt source A enable

IEB = Interrupt source B enable

IEC = Interrupt source C enable

ISA[2:0] = Interrupt source A (selected IRQ driven at J10):

Signal Name Location
000 = CT_OUT0 (J13.5) (default)
001 = CT_OUT1 (J13.6)
010 = CT_OUT2 (J13.11)
011 = IRQ_IN0 (J12.22)
100 = IRQ_IN1 (J9.22)
101 = IRQ_IN2 (J13.8)
110 = 8255 #1 Bit C0 (J12.31)
111 = 8255 #2 Bit C0 (J9.31)

ISB[2:0] = Interrupt source B (selected IRQ driven at J5):

Signal Name Location
000 = CT_OUT0 (J13.5) (default)
001 = CT_OUT1 (J13.6)
010 = CT_OUT2 (J13.11)
011 = IRQ_IN0 (J12.22)
100 = IRQ_IN1 (J9.22)
101 = IRQ_IN2 (J13.8)
110 = 8255 #1 Bit C0 (J12.31)
111 = 8255 #2 Bit C0 (J9.31)

ISC[2:0] = Interrupt source C (selected IRQ driven at J9):

Signal Name Location
000 = CT_OUT0 (J13.5) (default)
001 = CT_OUT1 (J13.6)
010 = CT_OUT2 (J13.11)
011 = IRQ_IN0 (J12.22)
100 = IRQ_IN1 (J9.22)
101 = IRQ_IN2 (J13.8)
110 = 8255 #1 Bit C0 (J12.31)
111 = 8255 #2 Bit C0 (J9.31)

LED[3:0] = LED drive source.

0000 = base address decode (default) *
0001 = Counter/Timer 0 Input (CI0)
0010 = Counter/Timer 1 Input (CI1)
0011 = Counter/Timer 2 Input (CI2)
0100 = Counter/Timer 0 Output
0101 = Counter/Timer 1 Output
0110 = Counter/Timer 2 Output
0111 = Interrupt Source A (ISA) *
1000 = IRQ_IN0
1001 = IRQ_IN1
1010 = IRQ_IN2
1011 = none
1100 = Interrupt Source B (ISB) *
1101 = Interrupt Source C (ISC) *
1110 = LED off always
1111 = LED on always
* LED minimum pulse size is approximately 0.016 seconds which support

9 Dry Contact, Open Collector or Open Drain Requirements

Due to bus-hold circuits buried into the buffer chips (near impossible to avoid) additional pull-ups are required to overdrive the bus hold features. Note that bus holds were implemented in these devices to eliminate the need for floating inputs to be tied high or low by holding the last known state of the input and thereby reducing overall power consumption and eliminating the need for external pull resistors.

Thus, in order to properly use the Tracer with dry contact inputs, open drain or open collector inputs additional external pull up resistor will be required as calculated R_pullup_max. Referring to the proper specifications we can calculate the maximum pull-up resistance value to overdrive the bus hold. The R_pullup_max can be a value less than or equal to the calculated R_pullup_max.

TRACER-DIO-3.3VIO

VCC = 3.3 volts

VIH_MIN = 1.5 volts

IBHHO = 500 uA

R_pullup_max <= (VCC - VIH_MIN) / IBHHO = (3.3 - 1.5) / 500 uA = 3.6 Kohm

Thus, a pull of 3.6 K ohms or less will be required to pull the input to a logic one.

TRACER-DIO-5VIO

VCC = 5.0 volts

VIH_MIN = 0.7 * VCC

IBHHO = 900 uA

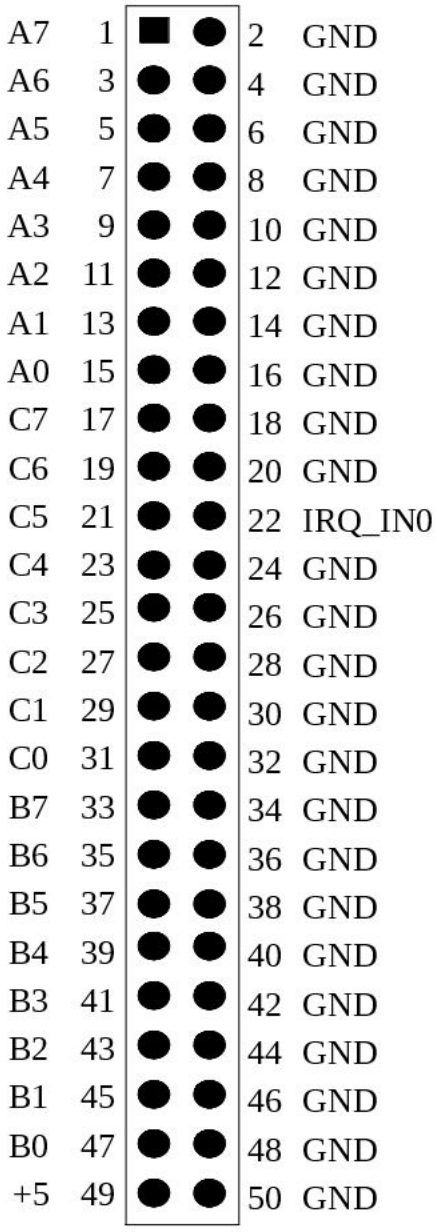
R_pullup_max <= (VCC - VIH_MIN) / IBHHO = (VCC - 0.7 * VCC) / IBHHO

R_pullup_max <= 0.3 * VCC / IBHHO = 0.3 * 5.0 / 900 uA = 1.67 Kohm

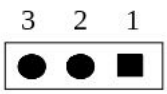
Thus, a pull of 1.6 K ohms or less will be required to pull the input to a logic one.

10 Connector Summary

Digital I/O Connector J12, 8255 #1



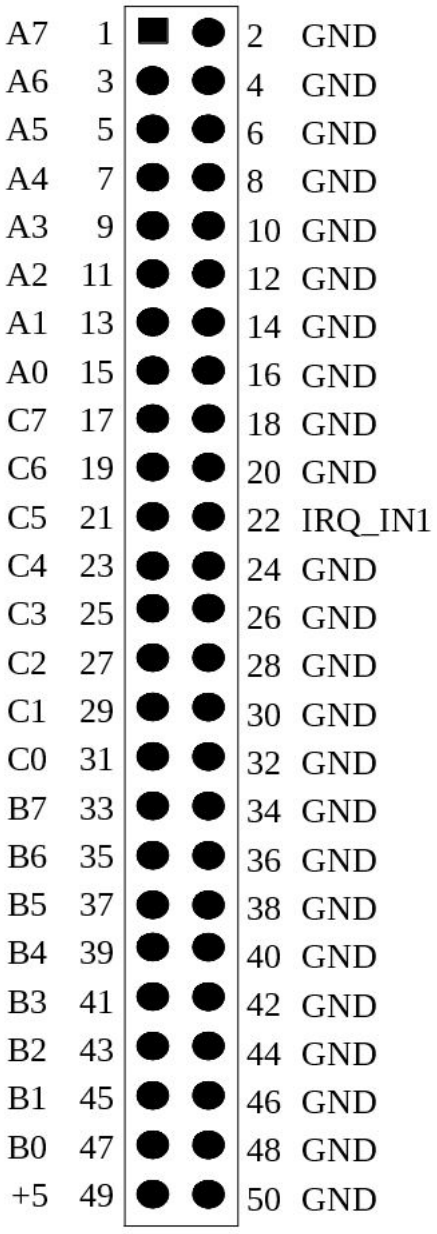
External IRQ Source 0 (IRQ_IN0) J5



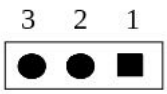
Jumper Position	Function
1-2	External Interrupt source 0 input at J12 pin 22 (J12.22)
2-3*	J12 pin 22 grounded (for opto 22 rack compatibility). External Interrupt Source 0 not available.

* FACTORY CONFIGURATION

Digital I/O Connector J9, 8255 #2



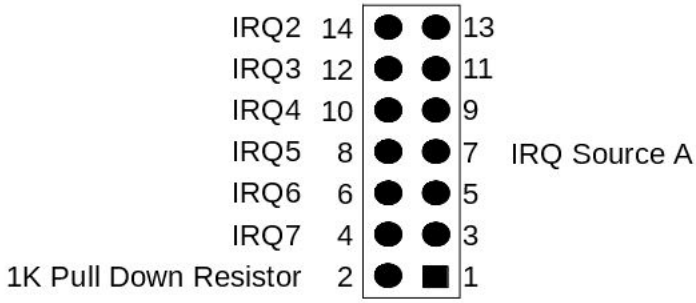
External IRQ Source 1 (IRQ_IN1) J7



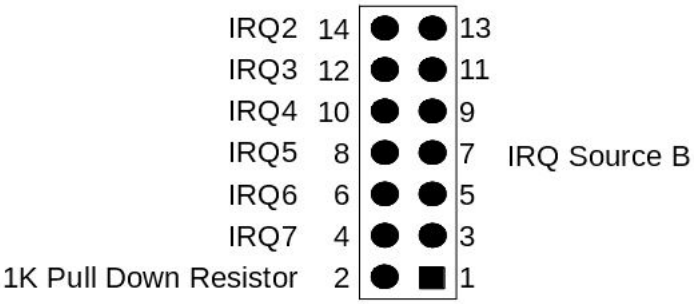
Jumper Position	Function
1-2	External Interrupt source 1 input at J9 pin 22 (J9.22)
2-3*	J9 pin 22 grounded (for opto 22 rack compatibility). External Interrupt Source 1 not available.

* FACTORY CONFIGURATION

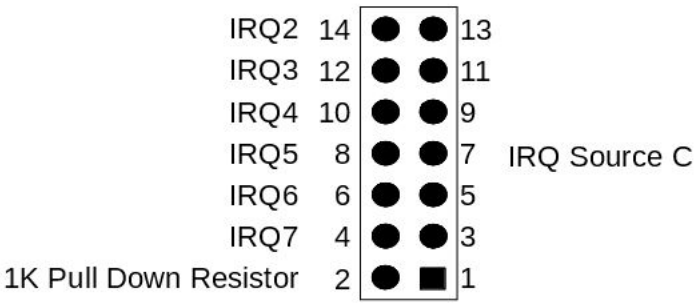
PC/104 IRQ Source A Connector J10



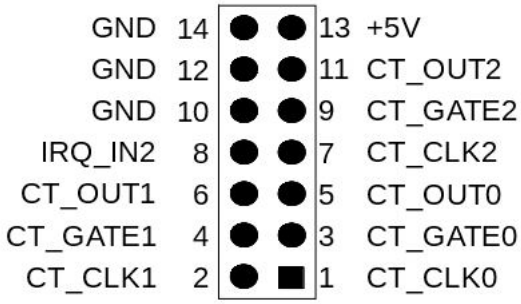
PC/104 IRQ Source B Connector J8



PC/104 IRQ Source C Connector J6



Counter Timer Connector J13



Name	Direction
CT_CLK0	Input to Tracer Board
CT_GATE0	Input to Tracer Board
CT_OUT0	Output from Tracer Board
CT_CLK1	Input to Tracer Board
CT_GATE1	Input to Tracer Board
CT_OUT1	Output from Tracer Board
CT_CLK2	Input to Tracer Board
CT_GATE2	Input to Tracer Board
CT_OUT2	Output from Tracer Board
IRQ_IN2	Additional interrupt input

11 Specification

Common specifications across all Tracer part numbers

General	Operating temperature range:	-40 to +85C
	Storage temperature range:	-55 to +125C
	Humidity:	0 to 95% non-condensing
	Power supply:	5.0 VDC ± 10%, 120mA typical (inputs/outputs unloaded)
	Interface:	PC/104 8-bit bus
	Mechanical dimensions:	PC/104 form factor
Digital I/O		
	Functionality:	82C55A, quantity of two
	Number of digital I/O lines:	48
	Direction:	All lines programmable for input or output in groups of eight
Counter/Timer	Functionality:	Compliant to the 82C54-2
	Counter/Timers:	Quantity of 3, each 16-bits
	Maximum input frequency:	40 MHz
	On-board oscillator:	50 MHz ±0.01% (100ppm) divided down to 4, 10, 20 MHz
Interrupt Configuration	Number of System Interrupts:	3
	Selectable interrupt levels:	IRQ2,IRQ3,IRQ4,IRQ5,IRQ6,IRQ7
	Pull-down resistor:	1K resistor selectable via jumper on each interrupt
MTBF Information		
	MIL-HDBK-217F (Ground benign) at 25^{O}C	Failure Rate = 1.3801 MTBF = 724,559.2 hours
	MIL-HDBK-217F (Ground benign) at 40^{O}C	Failure Rate = 2.0463 MTBF = 488,690.0 hours
	Telcordia SR-332 (Ground, Fixed, Controlled) at 25^{O}C	FR(90) = 1042.3965 MTBF = 959,327.88 hours
	Telcordia SR-332 (Ground, Fixed, Controlled) at 40^{O}C	FR(90) = 1308.3085 MTBF = 764,345.75 hours

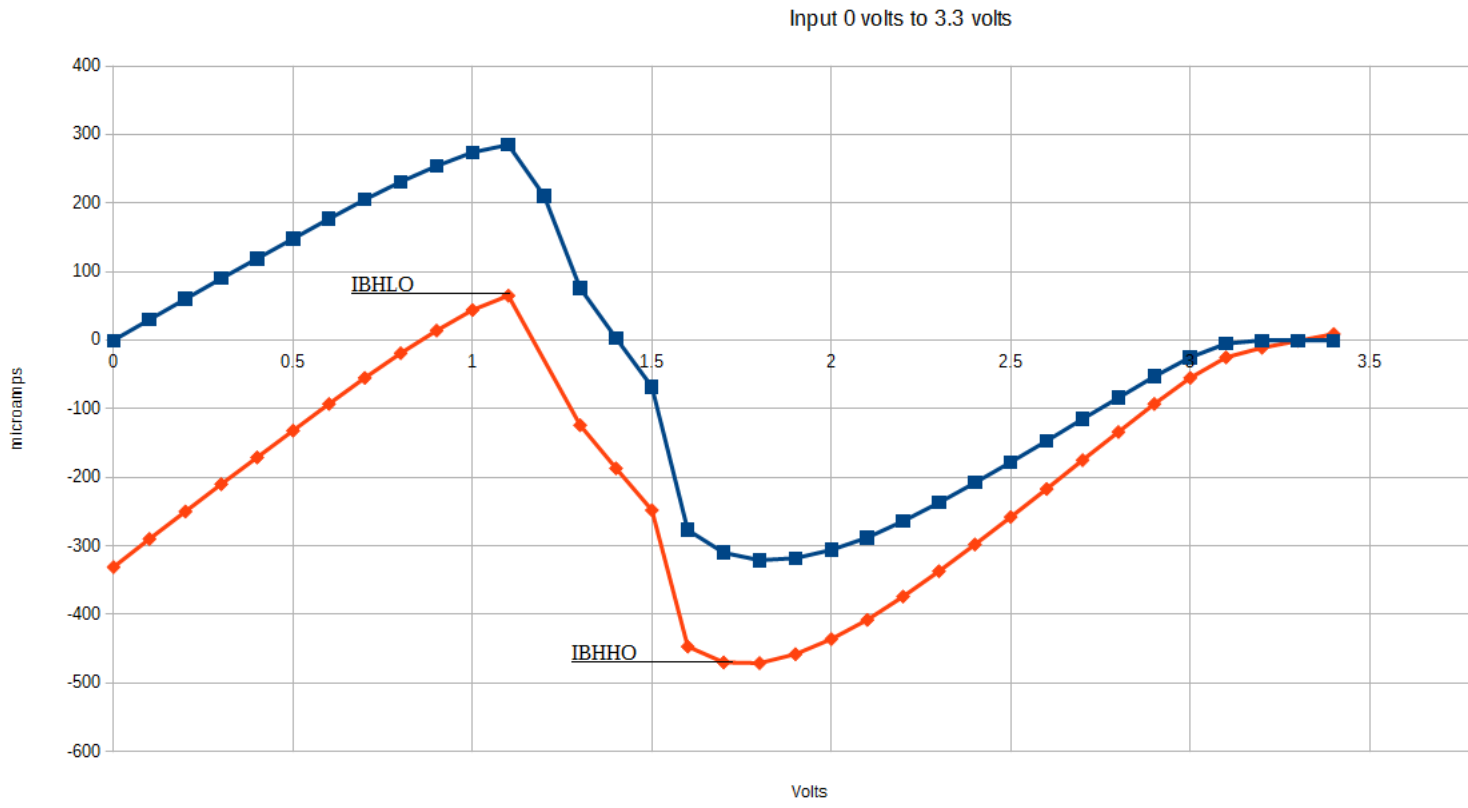
11.1 TRACER-DIO-3.3VIO

Specific digital I/O and counter/timer I/O electrical behavior

Input voltage:	
Compatibility:	TTL and LVTTL
Logic input low maximum (VIL_MAX):	0.8 volts
Logic input high minimum (VIH_MIN):	2.0 volts
Range:	0.0 to 5.0 volts (5 volt tolerant)
Input bus holds: Purpose: to keep unterminated inputs at known states and they are built-in to most all transceiver chips of this type.	YES
Bus hold high state overdrive current IBHHO (Require at least IBHHO sink current to drive input from high state to low state):	-500 uA
Bus hold low state overdrive current IBHLO (Require at least IBHLO source current to drive input from low state to high state):	500 uA
Pull-up resistor required to overdrive the bus hold: R_pullup_max = (VCC - VIH_MIN) / IBHHO	2.6 killiohms maximum. (*) Note: additional pull-up may be required depending on capacitive load.
Input current: Input current due to 10K legacy pull-ups to 3.3V and bus-holds	
Logic 0:	Transition high to low: -830 uA maximum DC state: 100 uA
Logic 1:	Transition low to high: -830 uA maximum DC state:
Output voltage:	
Compatibility:	TTL and LVTTL
Logic output low maximum (Vol):	0.55 volts @ 64 mA
Logic output high minimum (Voh):	2.0 volts @ -32 mA 2.4 volts @ -3 mA 3.3 volts @ -0 mA
Range:	0.0 to 3.3 volts as an output
Triastate voltage:	If load is tied to 5 volts it will float to 5 volts If no load, then I/O will be pulled to 3.3 volts

Buffer transceiver used: 74LVT245BQ,115 with I/O operating with 3.3V supply.
Built-in bus-holds.

Input Voltage versus Input Current



11.2 TRACER-DIO-5VIO

Specific digital I/O and counter/timer I/O electrical behavior

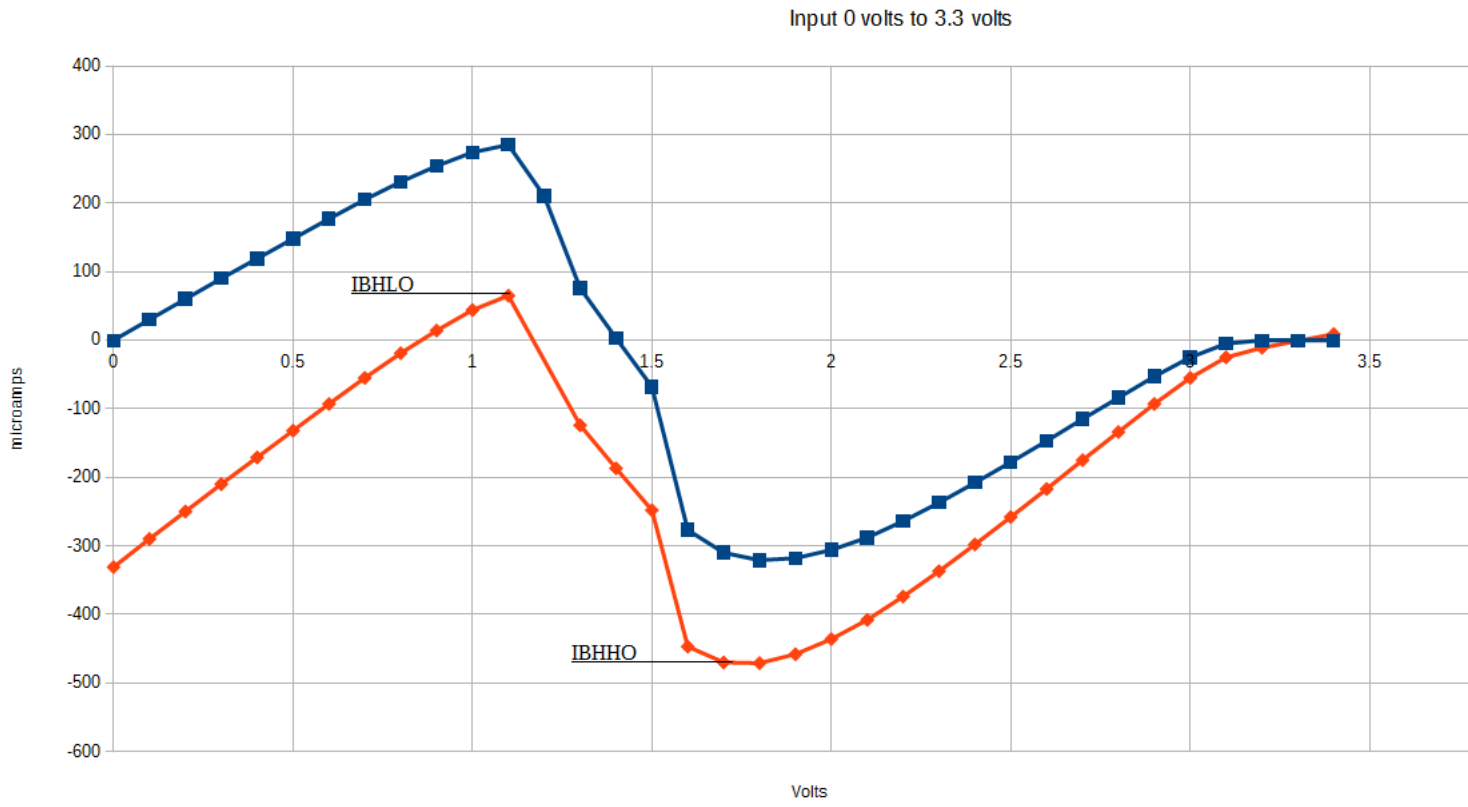
Input voltage:

Compatibility:	CMOS, TTL(*)
Logic input low maximum (VIL_MAX):	1.5 volts
Logic input high minimum (VIH_MIN = 0.7 * VCC):	3.5 volts
Range:	0.0 to 5.0 volts (full 5 volt range!)
Input bus holds:	YES

Purpose: to keep unterminated inputs at known states and they are built-in to most all transceiver chips of this type.

Bus hold high state overdrive current IBHHO (Require at least IBHHO sink current to drive input from high state to low state):	-500 uA
Bus hold low state overdrive current IBHLO (Require at least IBHLO source current to drive input from low state to high state):	500 uA
Pull-up resistor required to overdrive the bus hold: R_pullup_max = (VCC - VIH_MIN) / IBHHO	1.6 killiohms maximum. (*) Note: additional pull-up may be required depending on capacitive load.
Input current: Input current due to 10K legacy pull-ups to 5 volts and bus-holds	
Logic 0:	Transition low to high: -830 uA maximum DC state: -500 uA maximum at 0.0 volts
Logic 1:	Transition low to high: -830 uA maximum DC state: -150 uA maximum at 3.5 volts
Output voltage:	
Compatibility:	TTL
Logic output low maximum (VOL_MAX):	0.55 volts @ 64 mA
Logic output high minimum (VOH_MIN):	2.0 volts @ -32 mA 2.4 volts @ -3 mA 5.0 volts @ -0 mA
Range:	0.0 to 5.0 volts as an output (full 5 volt range!)
Triastate voltage:	If load is tied to 5 volts it will float to 5 volts If no load, then I/O will be pulled to 5 volts
Buffer transceiver used:	SN74LVCH8T245 with I/O operating with 5.0V supply.

Input Voltage versus Input Current



11.3 Valid Part Numbers

Valid Part Number	Description
TRACER-DIO-3.3VIO	RUGGEDIZED COTs PC/104 High Drive 48-line DIO and counter-timer module. Full 5V I/O Legacy compatible. This product is an update from our classic Tracer-E. This version provides safe 3.3 volt output swings and all inputs are 5 volt tolerant.
TRACER-DIO-5VIO	RUGGEDIZED COTs PC/104 High Drive 48-line DIO and counter-timer module. Safe 3.3 volt compatibility. This product is an update from our classic Tracer-E. This version provides true 5 volt output swings and accepts 5 volt inputs as well.

NOTE: some TRACER-DIO-5VIO were shipped using the part number TRACER-E-5VFR. In order to unify all part numbers now and into the future, part numbers were updated to be of the form TRACER-DIO-<I/O specifier>.

11.4 Revision Information

REVISION INFORMATION

Date	PCB Date Code	CPLD Date Code	FPGA Date Code	Description
October 13, 2016	160912	161011	161011	Original release of firmware
April 13, 2017	160912	161216	161116	Reorganization of firmware, no logical changes.
December 11, 2017	170908	171116	171116	Added M2 jumper functionality

12 Application Notes

12.1 Quadrature Decoder

Connecting a quadrature output incremental optical shaft encoder to the counter/timer input.

Wiring:	Phase A	CT_GATE1	J13.4
	Phase B	CT_CLK1	J13.2
	Common	GND	J13.14
	Power	+5V	J13.15

Counter/Timer Setup Resister:

CT_GATE1 inverted	True
CT_CLK1 inverted	False
CT_CLK1 source	CT_IN1
CT_GATE0 inverted	True
CT_GATE0 source	CT_GATE1
CT_CLK0 inverted	True
CT_CLK0 source	CT_IN1

```
Base_Address + 12 <= 0000 1001
Base_Address + 13 <= 1?01 1???
where ‘?’ is the configuration for Counter/Timer #2.

Software setup:

base_address = 0x300;
Counter/Timer Setup Register = 0x0000
CT0: Clock: Inverted=False, Source=CT_IN0
Gate: Inverter=False, Source=CT_GATE1
CT1: Clock: Inverted=False, Source=CT_IN1
Gate: Inverter=False, Source=CT_GATE1
CT2: Clock: Inverted=False, Source=CT_IN2
Gate: Inverter=False, Source=CT_GATE2
```

13 Limited Warranty

Unless altered by written agreement, Apex Embedded Systems LLC (APEX) warrants to the original purchaser for a period of one year from the date of original purchase, that the products shall be free from defects in material and workmanship. APEX's obligation under this warranty is limited to replacing or repairing, at its option and its designated site, any products (except consumables) within the warranty period that are returned to APEX in the original shipping container(s) with an APEX RMA number referenced on the shipping documents.

This warranty will not apply to products that have been misused, abused, or altered. This warranty will not apply to prototypes of any kind, engineering services, software or products under pre-release status. Any returns must be

supported by a Return Material Authorization (RMA) number issued by APEX. APEX reserves the right to refuse delivery of any shipment containing any shipping carton which does not have an RMA number displayed on the outside.

Purchaser shall prepay transportation to APEX's location. If returned parts or products are repaired under the terms of this warranty, APEX will pay return transportation charges. Allow six (6) to eight (8) weeks for warranty repairs.

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