Summit

PC/104 DDA06/16 Compatible

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Apex Embedded Systems

Reference Manual

Summit Reference Manual

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Support Policy

General Support Policy.

We support all hardware products for a period of 3 months from time of delivery. See limited warranty terms.

Recommended sequence in obtaining customer support

Review user manuals for additional information not found in demo software.

Go to our website at www.apexembedded.com/support.html.

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Continued Success,

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Caution

A discharge of static electricity from your hands can seriously damage certain electrical components on any circuit board. Before handling any board, discharge static electricity from yourself by touching a grounded conductor such as your computer chassis (your computer must be turned off). Whenever you handle a board, hold it by the edges and avoid touching any board components or cable connectors.

Chapter 1

Benefits and Features

The Stratus provides high functionality while making life a little easier

Executive Summary

What is the Summit?

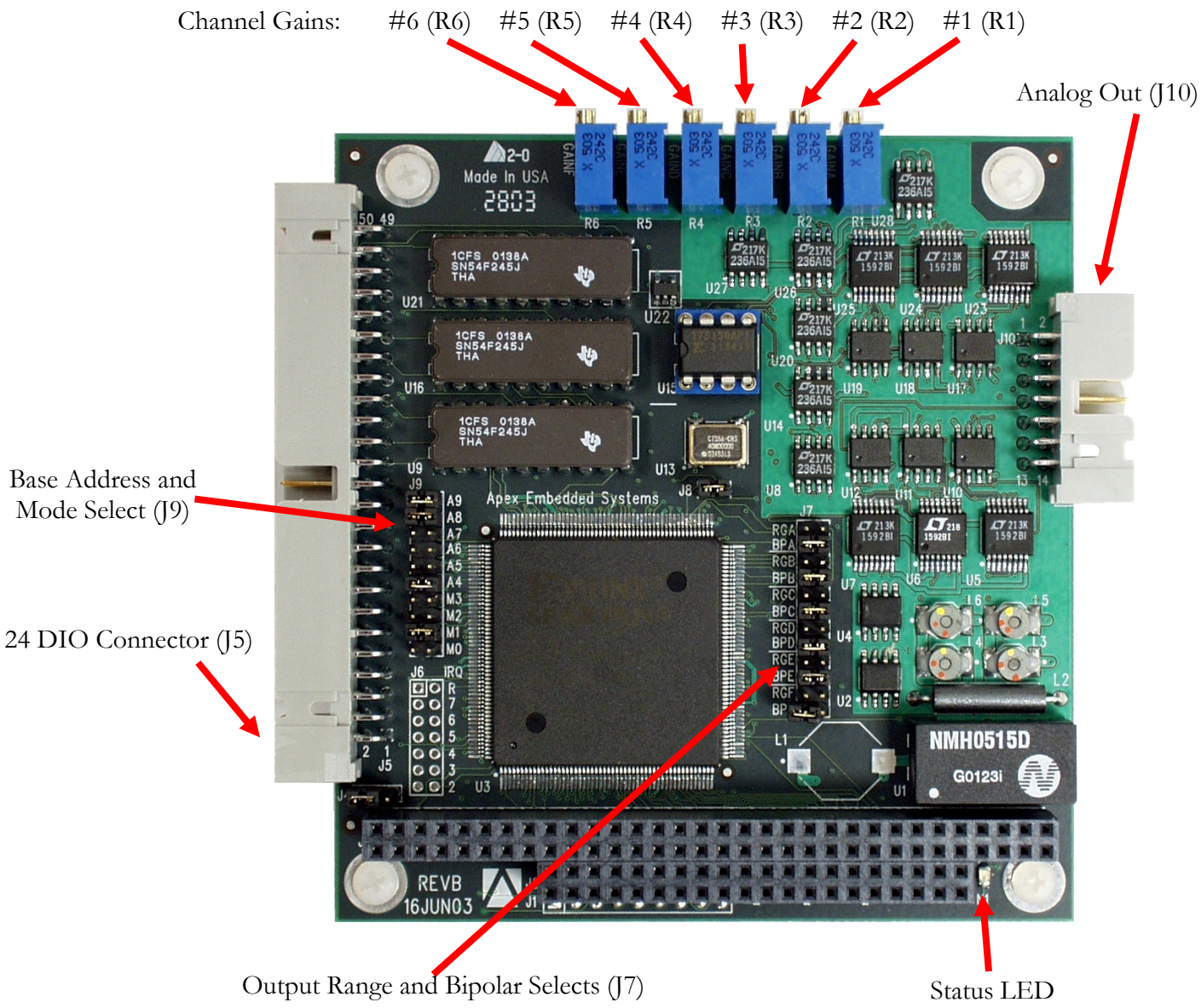
The Summit is a six channel analog output card with 16-bit resolution. In addition, the Summit provides 24-lines of high current digital I/O. It is designed for use in systems where high reliability is of utmost importance while operating in harsh environments.

What are the Benefits to using the Summit? The Summit has the following features and benefits:

- Compatible with DDA06/16 for using existing drivers
- 16-bit data write operations double effective PC/104 bus bandwidth
- DAC updates through a variety of methods including an external TTL input
- Use REP INSW (286 or higher CPU) to read-in blocks of ADC data from FIFO further increasing bandwidth and reducing complexity.
- On-board LED to indicate that the Summit is being addressed. By observing the LED you can quickly determine system activity.
- Polarized locking I/O connector. This eliminates board failures due to incorrect connector orientation.
- High-current outputs 65mA sink, 15mA source. This is true even while operating at high temperatures.
- LED Status indicator. Useful in determining general status and in system debugging. A wide variety of signals can be routed to the LED via software selection.
- 8255 Software compatible interface structure. The hardware provides one 8255 compatible I/O ports that provide 24 lines of general purpose I/O.

- Direct interfacing to OPTO-22's isolated I/O racks. Digital I/O connectors organized to allow direct connection to OPTO-22's isolated I/O racks including the G4 series, the PB16-H, PB16-J, PB16-K, PB16-L, PB8H and the PB24HQ.
- Industrial temperature range from -40°C to +85°C
- No tantalum capacitors or electrolytic capacitors used in the design
- Single +5V supply operation

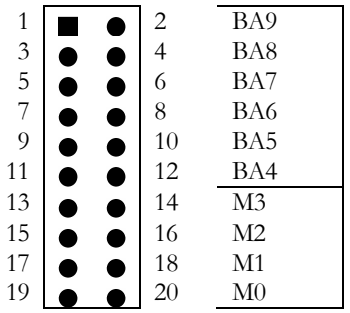
Photo



Chapter 2

Hardware Configuration

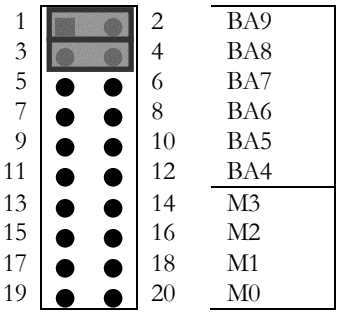
Base Address and Configuration



1	2	BA9		
3	4	BA8		
5	6	BA7	Base Address	
7	8	BA6		
9	10	BA5		
11	12	BA4		
13	14	M3		
15	16	M2	Mode Selection	
17	18	M1		
19	20	M0		

Example Base Address

Base Address = 768 or 0x300 ($11\ 0000\ 0000_2$)



1	2	BA9		
3	4	BA8		
5	6	BA7	Base Address	
7	8	BA6		
9	10	BA5		
11	12	BA4		
13	14	M3		
15	16	M2	See compatibility selection and	
17	18	M1	Extended functions table below.	
19	20	M0		

Base Address Table

Base Address	BA9	BA8	BA7	BA6	BA5	BA4
0x220	1	0	0	0	1	0
0x240	1	0	0	1	0	0
0x250	1	0	0	1	0	1
0x260	1	0	0	1	1	0
0x280	1	0	1	0	0	0
0x290	1	0	1	0	0	1
0x2A0	1	0	1	0	1	0
0x2B0	1	0	1	0	1	1
0x2C0	1	0	1	1	0	0
0x2D0	1	0	1	1	0	1
0x2E0	1	0	1	1	1	0
0x2F0	1	0	1	1	1	1
*0x300	1	1	0	0	0	0
0x310	1	1	0	0	0	1
0x320	1	1	0	0	1	0
0x330	1	1	0	0	1	1
0x340	1	1	0	1	0	0
0x350	1	1	0	1	0	1
0x360	1	1	0	1	1	0
0x370	1	1	0	1	1	1
0x380	1	1	1	0	0	0
0x390	1	1	1	0	0	1
0x3A0	1	1	1	0	1	0
0x3B0	1	1	1	0	1	1
0x3C0	1	1	1	1	0	0
0x3D0	1	1	1	1	0	1
0x3E0	1	1	1	1	1	0
0x3F0	1	1	1	1	1	1

Note: 1 = Jumper installed, 0 = Jumper not installed.

* Factory Default

Compatibility Selection and Extended Functions

Function	Mode	M3	M2	M1	M0
* DDA06 16-bit compatibility: - DAC update: simultaneous updating by reading any DAC register. - DAC status: not available	0	X	0	0	0
DAC Status Registers - DAC update: simultaneous updating by reading at 0x0F register. - DAC status: read at MSB of each DAC	1	X	0	0	1
DDA06 16-bit compatibility: - DAC update: individual update by writing to MSB of DAC register - DAC status: read at MSB of each DAC	2	X	0	1	0
DDA06 16-bit compatibility: - DAC update: External simultaneous strobe, J5.22. Jumper J4.1 & J4.2 shorted. Rising edge detection. - DAC status: read at MSB of each DAC	3	X	0	1	1
DDA06 16-bit compatibility: - DAC update: External simultaneous strobe, J5.22. Jumper J4.1 & J4.2 shorted. Falling edge detection. - DAC status: read at MSB of each DAC	4	X	1	0	0
Reserved	5	1	X	X	X

Note: 1 = Jumper installed, 0 = Jumper not installed.
* Factory Default

When using the Summit with the Stratus-X board and its' SS&H output, you will want to use Summit mode-3 for updating the DAC outputs just after the last ADC channel is sampled (or just before the first channel sample is taken). Use Summit mode-4 for updating the DAC outputs after the ADC first channel is sampled (this is useful if you are utilizing an external simultaneous sample and hold board).

Note: When J5 pin 22 is configured as a DAC_STROBE, it is pulled up with a 10Kohm resistor.

High Vibration Environments

Apex offers factory installed surface mount zero ohm resistors to replace all jumpers.

Chapter 3

Register Set

Register Set Summary

Offset (Decimal)	Offset (Hex)	Write Register	Read Register
0	00	DAC Channel-A LSB	ISU (Mode 0 only), otherwise None
1	01	DAC Channel-A MSB (update channel-A)	ISU (Mode 0 only), otherwise DAC-A Status
2	02	DAC Channel-B LSB	ISU (Mode 0 only), otherwise None
3	03	DAC Channel-B MSB (update channel-B)	ISU (Mode 0 only), otherwise DAC-B Status
4	04	DAC Channel-C LSB	ISU (Mode 0 only), otherwise None
5	05	DAC Channel-C MSB (update channel-C)	ISU (Mode 0 only), otherwise DAC-C Status
6	06	DAC Channel-D LSB	ISU (Mode 0 only), otherwise None
7	07	DAC Channel-D MSB (update channel-D)	ISU (Mode 0 only), otherwise DAC-D Status
8	08	DAC Channel-E LSB	ISU (Mode 0 only), otherwise None
9	09	DAC Channel-E MSB (update channel-E)	ISU (Mode 0 only), otherwise DAC-E Status
10	0A	DAC Channel-F LSB	ISU (Mode 0 only), otherwise None
11	0B	DAC Channel-F MSB (update channel-F)	ISU (Mode 0 only), otherwise DAC-F Status
12	0C	8255 Port A Outputs	8255 Port A Inputs
13	0D	8255 Port B Outputs	8255 Port B Inputs
14	0E	8255 Port C Outputs	8255 Port C Inputs
15	0F	8255 Configure	ISU (Mode 1 only), otherwise None

Notes:
(1) 1 = Jumper installed, 0 = Jumper not installed.
(2) ISU == Initiate Simultaneous Update

DAC Data Registers

Base Address + 0 **DAC Channel-A Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Base Address + 1 **DAC Channel-A High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

Base Address + 2 **DAC Channel-B Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Base Address + 3 **DAC Channel-B High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8

Base Address + 4 **DAC Channel-C Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Base Address + 5 **DAC Channel-C High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8

Base Address + 6 **DAC Channel-D Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Base Address + 7 **DAC Channel-D High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DD15	DD14	DD13	DD12	DD11	DD10	DD9	DD8

Base Address + 8 **DAC Channel-E Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0

Base Address + 9 **DAC Channel-E High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DE15	DE14	DE13	DE12	DE11	DE10	DE9	DE8

Base Address + 10 **DAC Channel-F Low Byte (LSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0

Base Address + 11 **DAC Channel-F High Byte (MSB)** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
DF15	DF14	DF13	DF12	DF11	DF10	DF9	DF8

Bit Definitions

DA[15:0]	=	DAC Channel-A data. DA0 is the least significant bit and DA15 is the most significant data bit.
DB[15:0]	=	DAC Channel-B data. DB0 is the least significant bit and DB15 is the most significant data bit.
DC[15:0]	=	DAC Channel-C data. DC0 is the least significant bit and DC15 is the most significant data bit.
DD[15:0]	=	DAC Channel-D data. DD0 is the least significant bit and DD15 is the most significant data bit.
DE[15:0]	=	DAC Channel-E data. DE0 is the least significant bit and DE15 is the most significant data bit.
DF[15:0]	=	DAC Channel-F data. DF0 is the least significant bit and DF15 is the most significant data bit.

DAC Updates

The Summit has several methods of DAC updating depending on the mode jumper selection as shown in the Compatibility Selection and Extended Functions Table.

Jumper Settings

The results of changing jumper settings at J7 will only take affect after a DAC update has occurred.

Data Transfer

Data transfer to a DAC channel can be performed in 8-bit or 16-bit I/O write transactions. The 8-bit DAC registers can be written 8-bits at a time or 16-bits by writing the data as a 16-bit I/O transaction (Examples: "out dx, ax" or "outpw(base_address+4, dac_value)").

DAC Outputs at Power-up

At power-up or reset the DAC outputs are at set to zero volts.

The DAC outputs are always enabled and available for use.

Software Examples

Examples of how to write to the DAC output registers.

8-Bit Writes in C/C++:

```
unsigned int dac_value;
...
outportb( base_address+0, dac_value & 0xFF );
outportb( base_address+1, dac_value >> 8 );
...
```

16-Bit Write in C/C++:

```
unsigned int dac_value;
...
outpw( base_address+0, dac_value );
...
```

Output Voltage Conversion

Output Range	Resolution	Input Voltage		Binary Code	
		-FS	+FS	-Full Scale	+Full Scale
± 10V	305uV	-10	+10	0000 0000 0000 0000	1111 1111 1111 1111
± 5V	153uV	-5	+5	0000 0000 0000 0000	1111 1111 1111 1111
0-10V	153uV	0.00	+10	0000 0000 0000 0000	1111 1111 1111 1111
0-5V	76uV	0.00	+5	0000 0000 0000 0000	1111 1111 1111 1111

DAC Status Registers

The DAC Status Register is available in all modes except mode zero. The two least significant bits, BPx and RGx, reflect the DAC jumper settings. This is very useful for software in determining how to convert voltage values to the raw DAC output values. BSYx is a busy bit indicating that the internal state machine is busy writing data to the DAC which is completed in less than five microseconds.

Base Address + 1 **DAC Channel-A Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYA	0	0	0	0	0	BPA	RGA

Base Address + 3 **DAC Channel-B Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYB	0	0	0	0	0	BPB	RGB

Base Address + 5 **DAC Channel-C Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYC	0	0	0	0	0	BPC	RGC

Base Address + 7 **DAC Channel-D Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYD	0	0	0	0	0	BPD	RGD

Base Address + 9 **DAC Channel-E Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYE	0	0	0	0	0	BPE	RGE

Base Address + 11 **DAC Channel-F Status Byte (MSB)** **Read**

D7	D6	D5	D4	D3	D2	D1	D0
BSYF	0	0	0	0	0	BPF	RGF

Bit Definitions

BSYx = DAC Channel-x Busy Status. If busy is a one then the internal state machine is busy sending a new value to the DAC. This occurs in about 5 microseconds.

RGx = DAC Channel-x Range Jumper.
0 = 5V range, no jumper installed
1 = 10V range, jumper installed

BPx = DAC Channel-x Bipolar Jumper.
0 = Unipolar output, no jumper installed
1 = Bipolar output, jumper installed

8255 Register Set

8255 Registers

Detailed register information for 8255 device #1. Both bit names and associated connector placement are shown where applicable (i.e. ref.pin#).

Base + 12 **8255 Port A Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1A7	1A6	1A5	1A4	1A3	1A2	1A1	1A0
Associated Connector Pins:							
J5.1	J5.3	J5.5	J5.7	J5.9	J5.11	J5.13	J5.15

Base + 13 **8255 Port B Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
Associated Connector Pins:							
J5.33	J5.35	J5.37	J5.39	J5.41	J5.43	J5.45	J5.47

Base + 14 **8255 Port C Register** **Read/Write**

D7	D6	D5	D4	D3	D2	D1	D0
1C7	1C6	1C5	1C4	1C3	1C2	1C1	1C0
Associated Connector Pins:							
J5.17	J5.19	J5.21	J5.23	J5.25	J5.27	J5.29	J5.31

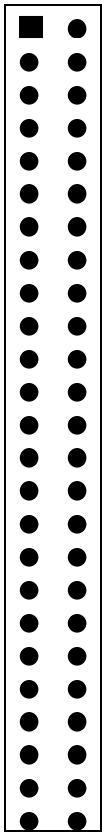
Base + 15 **8255 Configuration Register** **Write**

D7	D6	D5	D4	D3	D2	D1	D0
Mode Set	Group A				Group B		
	M3	M2	A	CH	M1	B	CL

8255 Configuration codes valid for the Summit. Only Mode 0 is supported.

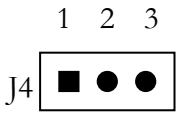
Port Direction					Hex Value	Decimal Value
A	CH	CL	B			
IN	IN	IN	IN		0x9B	155
IN	IN	IN	OUT		0x99	153
IN	OUT	OUT	IN		0x92	146
IN	OUT	OUT	OUT		0x90	144
OUT	IN	IN	IN		0x8B	139
OUT	IN	IN	OUT		0x89	137
OUT	OUT	OUT	IN		0x82	130
OUT	OUT	OUT	OUT		0x80	128

Digital I/O Connector J5.



A7	1	2	GND	
A6	3	4	GND	
A5	5	6	GND	
A4	7	8	GND	
A3	9	10	GND	
A2	11	12	GND	
A1	13	14	GND	
A0	15	16	GND	
C7	17	18	GND	
C6	19	20	GND	
C5	21	22	GND / DAC_STROBE	
C4	23	24	GND	
C3	25	26	GND	
C2	27	28	GND	
C1	29	30	GND	
C0	31	32	GND	
B7	33	34	GND	
B6	35	36	GND	
B5	37	38	GND	
B4	39	40	GND	
B3	41	42	GND	
B2	43	44	GND	
B1	45	46	GND	
B0	47	48	GND	
+5V	49	50	GND	

External DAC Trigger J4



Jumper Position	Function
1-2*	External DAC simultaneous strobe input at J5 pin 22 (J5.22)
2-3	J5 pin 22 grounded (for OPTO 22 rack compatibility) External Interrupt Source 0 not available.

* Factory Default

Note: When J5 pin 22 is configured as a DAC_STROBE, it is pulled up with a 10Kohm resistor.

Chapter 4

Calibration

Calibration made easy

Perform the following procedure to adjust DAC channel-n:

1. Select the desired output range by adjusting jumper settings at J7.
2. Output full scale by writing 65535 (0xFFFF) to the DAC output register.
3. Adjust potentiometer GAIN(n) until the desired full scale is reached. For example: if you have selected 0-5V output, then adjust the DAC output for 5.0000 volts.
4. Calibration is complete.

Chapter 5

Connector Summary

I/O Connector J10

DAC CH-A Output	1	2	Analog Ground (AGND)
DAC CH-B Output	3	4	Analog Ground (AGND)
DAC CH-C Output	5	6	Analog Ground (AGND)
DAC CH-D Output	7	8	Analog Ground (AGND)
DAC CH-E Output	9	10	Analog Ground (AGND)
DAC CH-F Output	11	12	Analog Ground (AGND)
No Connection	13	14	No Connection

J8

DAC Range Settings J7

RGA	1	2	DAC-A Range
BPA	3	4	DAC-A Bipolar
RGB	5	6	DAC-B Range
BPB	7	8	DAC-B Bipolar
RGC	9	10	DAC-C Range
BPC	11	12	DAC-C Bipolar
RGD	13	14	DAC-D Range
BPD	15	16	DAC-D Bipolar
RGE	17	18	DAC-E Range
BPE	19	20	DAC-E Bipolar
RGF	21	22	DAC-F Range
BPF	23	24	DAC-F Bipolar

J7

BPA	RGA	DAC Channel-A Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

BPB	RGB	DAC Channel-B Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

BPC	RGC	DAC Channel-C Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

BPD	RGD	DAC Channel-D Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

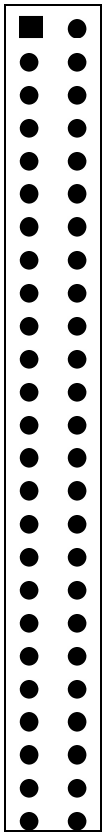
BPE	RGE	DAC Channel-E Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

BPF	RGF	DAC Channel-F Range
0	0	0 to +5 Volts *
0	1	0 to +10 Volts
1	0	-5 to +5 Volts
1	1	-10 to +10 Volts

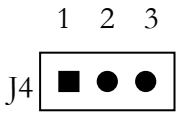
* Factory Default
Note: 1 = Jumper installed, 0 = Jumper not installed.

Digital I/O Connector J5.



A7	1	2	GND	
A6	3	4	GND	
A5	5	6	GND	
A4	7	8	GND	
A3	9	10	GND	
A2	11	12	GND	
A1	13	14	GND	
A0	15	16	GND	
C7	17	18	GND	
C6	19	20	GND	
C5	21	22	GND / DAC_STROBE	
C4	23	24	GND	
C3	25	26	GND	
C2	27	28	GND	
C1	29	30	GND	
C0	31	32	GND	
B7	33	34	GND	
B6	35	36	GND	
B5	37	38	GND	
B4	39	40	GND	
B3	41	42	GND	
B2	43	44	GND	
B1	45	46	GND	
B0	47	48	GND	
+5V	49	50	GND	

External DAC Trigger J4



Jumper Position	Function
1-2*	External DAC trigger input at J5 pin 22 (J5.22)
2-3	J5 pin 22 grounded (for OPTO 22 rack compatibility) External Interrupt Source 0 not available.

* Factory Default

Note: When J5 pin 22 is configured as a DAC_STROBE, it is pulled up with a 10Kohm resistor.

Chapter 6

Specification

Analog Outputs

Resolution	16-bits
Number of Channels	6 DACs
Output Voltage Ranges	±10V, ±5V, 0-10V, 0-5V. Maximum current to 5 milliamps per channel. Each channel independently configurable by jumpers.
Output Coupling	DC
Output Impedance	less than one ohm (0.7Ω typical), from 0 to ±5mA
Output short-circuit	±35mA continuous
Offset Error	less than 8 LSB
Gain Error	Adjustable to 0 LSB by potentiometer
Differential non-linearity	±1 LSB maximum
Settle Time	10 microseconds
Integral non-linearity	±1 LSB maximum
DAC Update	Selectable by jumper: (1) Simultaneous by reading any DAC Register, (2) Simultaneous updating by reading at base_address+0xF register, (3) Individual by writing to DAC MSB register, and (4) Simultaneous via external Strobe.
Monotonicity Guaranteed	

Digital I/O Circuitry

Functionality	82C55A, quantity of two
Number of digital I/O lines	48
Direction	All lines programmable for input or output in groups of eight
Input Voltage, all inputs:	TTL compatible
Low	-0.5V min, 0.8V max
High	2.0V min, 5.5V max
Current	5uA max (high), -1.2mA max (low)
Output Voltage, all outputs:	TTL compatible
Low	0.5 V max @ 24mA, 0.55V max @ 64mA
High	2.4 V @ - 3mA, 2.0V @ -15mA
Pull up resistors	10K on all digital I/O

General

Operating temperature range	-40 to 85°C
Storage temperature range	-55 to 125°C
Factory Calibration	Full NIST Traceable
Humidity	0 to 95% non-condensing

Power Supply	+5 VDC ± 5% at 550mA
Interface	PC/104 8- or 16-bit

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